FIG. 1

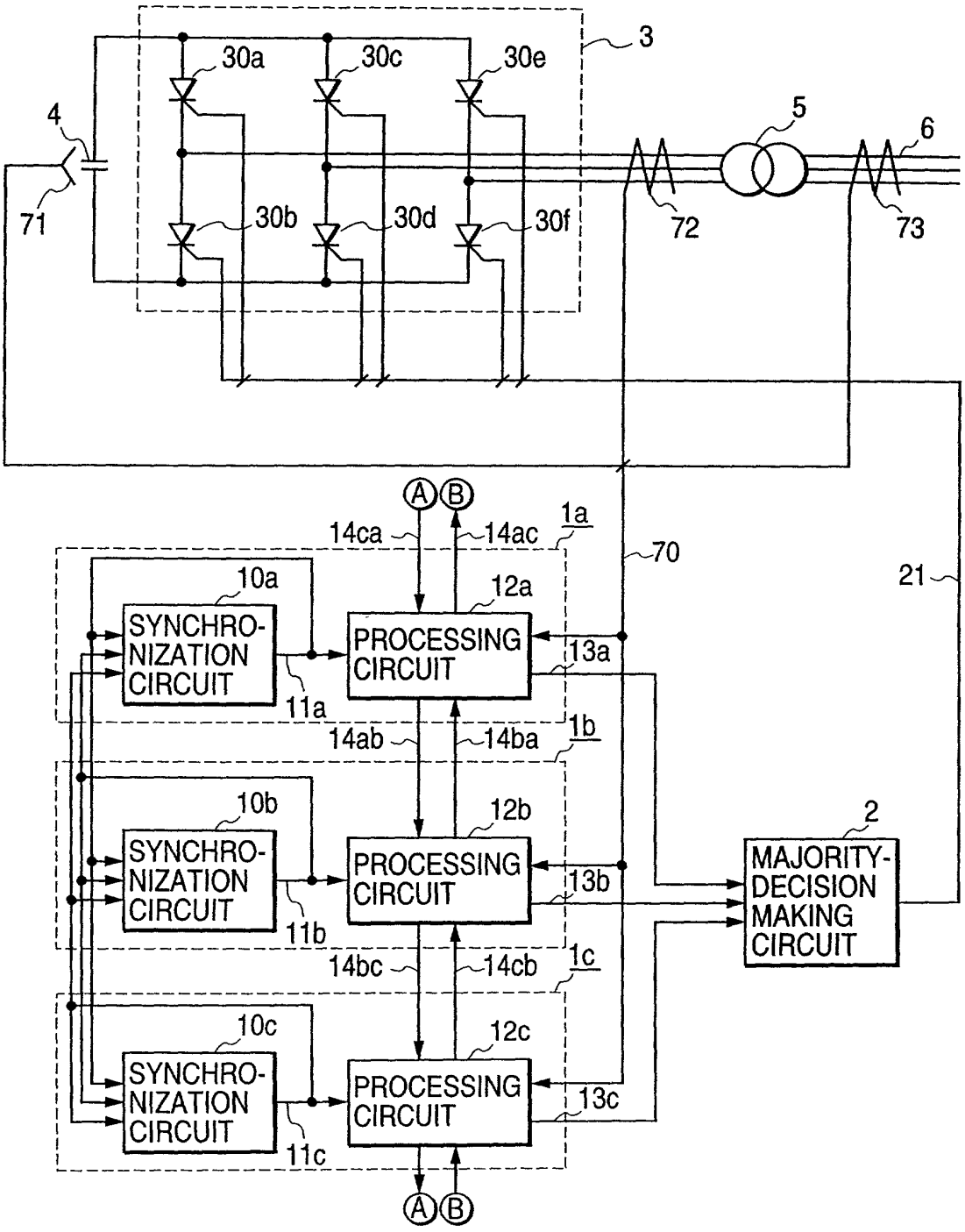

3
30a
30c
30e
4
5
6
71
30b
30d
30f
72
73
A
B
14ca
14ac
1a
70
21
10a
12a
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13a
11a
14ab
14ba
1b
10b
12b
2
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13b
MAJORITY-DECISION MAKING CIRCUIT
11b
14bc
14cb
1c
10c
12c
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13c
11c
A
B

FIG. 2

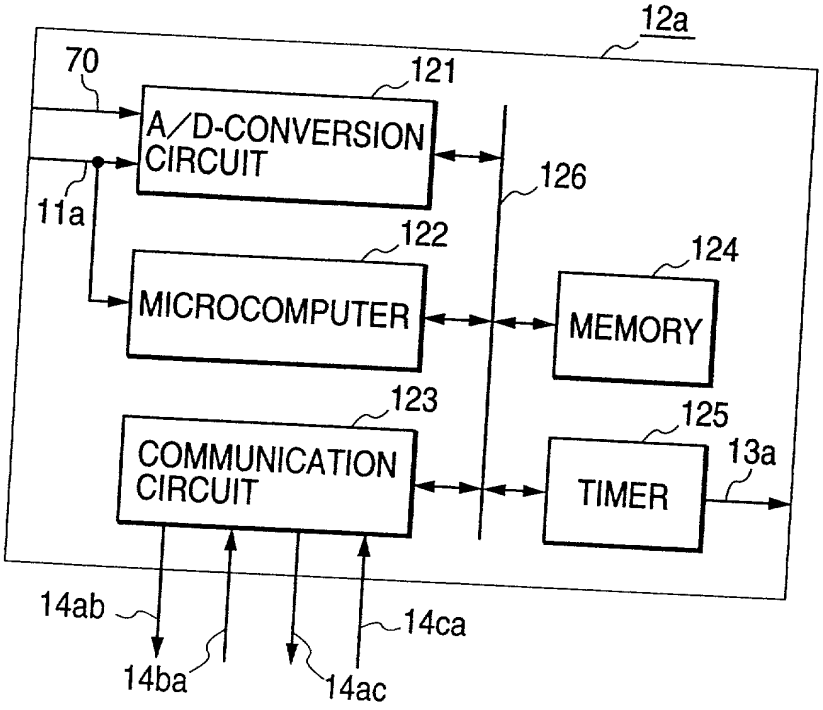

12a
70
121
A/D-CONVERSION CIRCUIT
11a
126
122
MICROCOMPUTER
124
MEMORY
123
COMMUNICATION CIRCUIT
125
TIMER
13a
14ab
14ba
14ac
14ca

FIG. 4

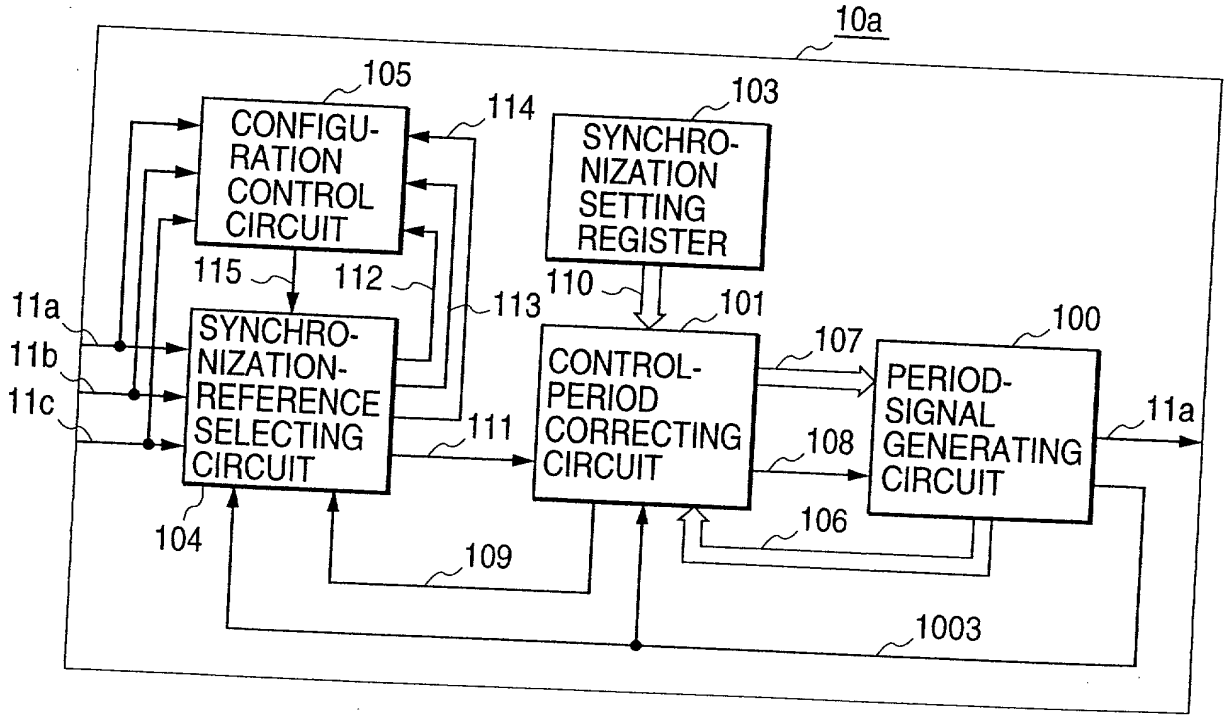

10a
105
CONFIGU-RATION CONTROL CIRCUIT
114
103
SYNCHRO-NIZATION SETTING REGISTER
115
112
110
113
101
11a
11b
11c
SYNCHRO-NIZATION-REFERENCE SELECTING CIRCUIT
CONTROL-PERIOD CORRECTING CIRCUIT
107
100
PERIOD-SIGNAL GENERATING CIRCUIT
11a
111
108
104
106
109
1003

FIG. 3(a)

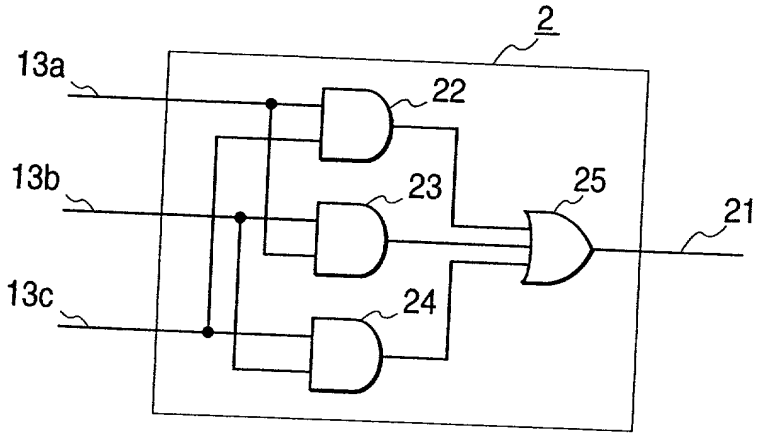

2
13a
13b
13c
22
23
24
25
21

FIG. 3(b)

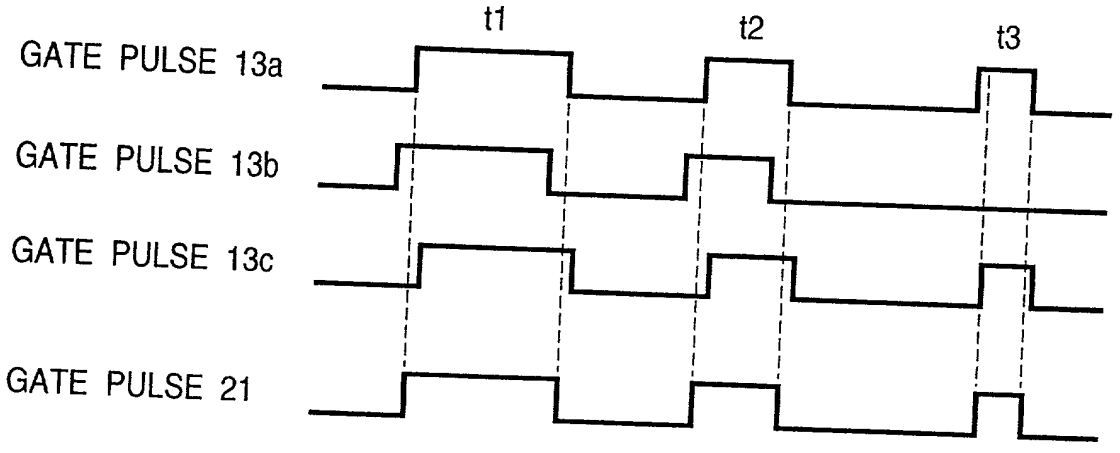

t1
t2
t3
GATE PULSE 13a
GATE PULSE 13b
GATE PULSE 13c
GATE PULSE 21

FIG. 5

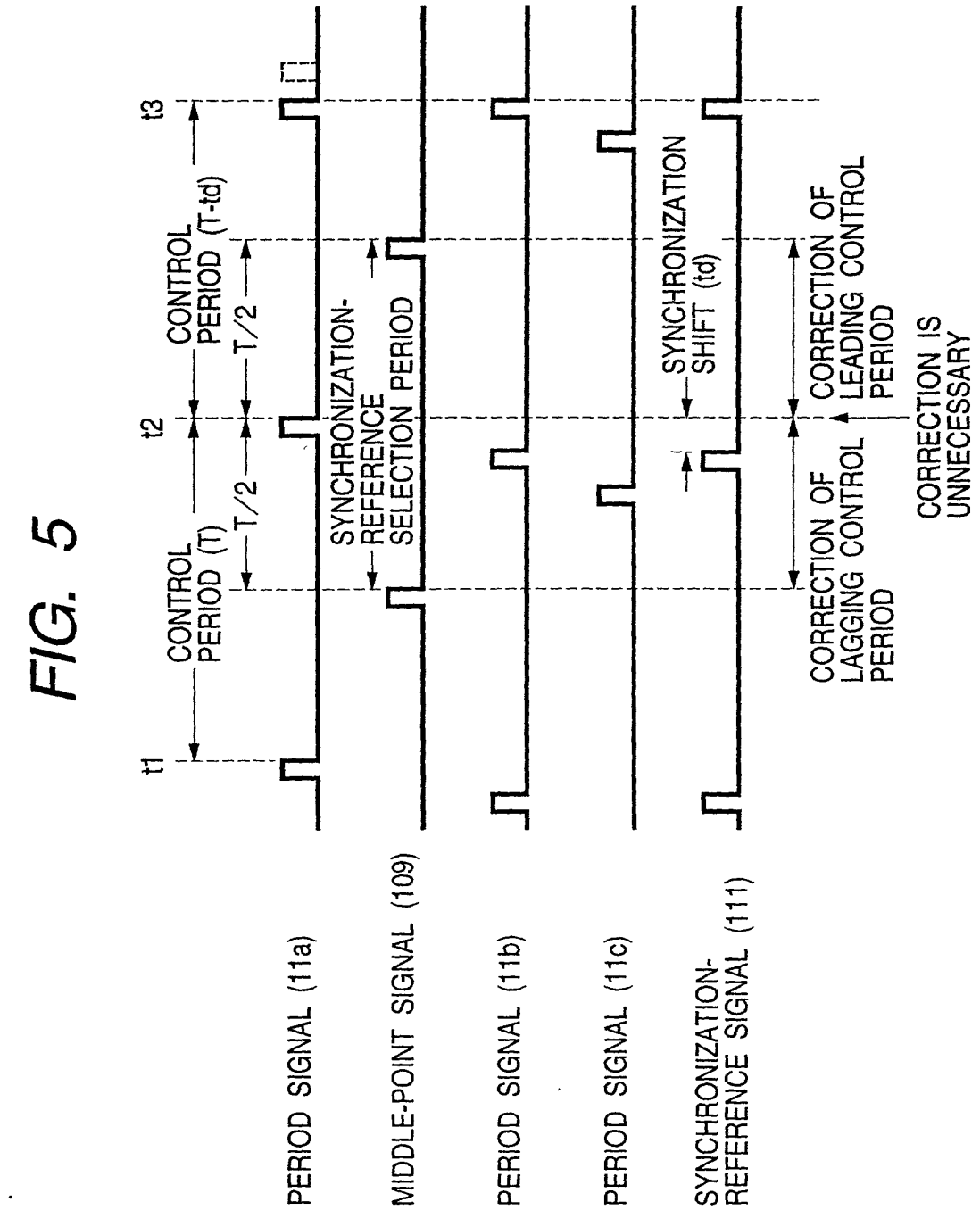

t1
t2
t3
CONTROL PERIOD (T)
T/2
T/2
CONTROL PERIOD (T-td)
SYNCHRONIZATION-REFERENCE SELECTION PERIOD
SYNCHRONIZATION SHIFT (td)
CORRECTION OF LAGGING CONTROL PERIOD
CORRECTION OF LEADING CONTROL PERIOD
CORRECTION IS UNNECESSARY
PERIOD SIGNAL (11a)
MIDDLE-POINT SIGNAL (109)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
SYNCHRONIZATION-REFERENCE SIGNAL (111)

FIG. 6

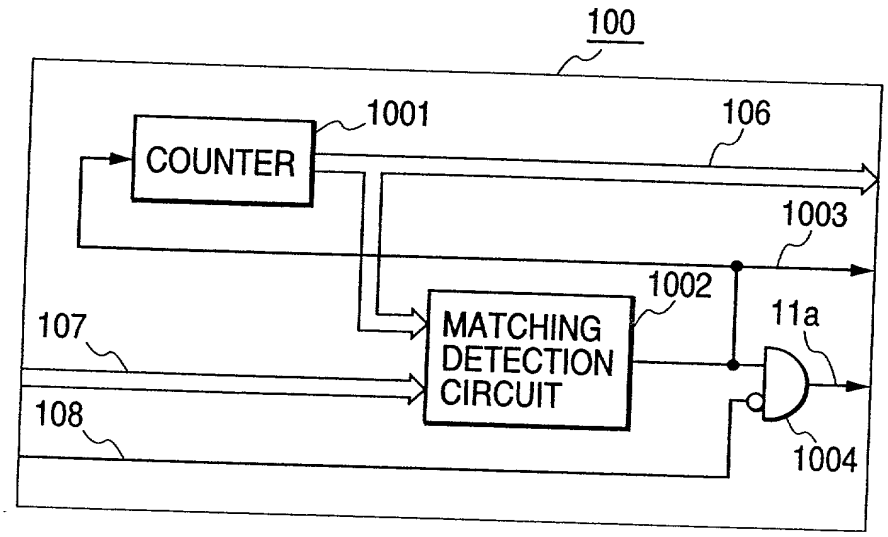

100
1001
106
COUNTER
1003
1002
11a
107
MATCHING
DETECTION
CIRCUIT
108
1004

FIG. 7

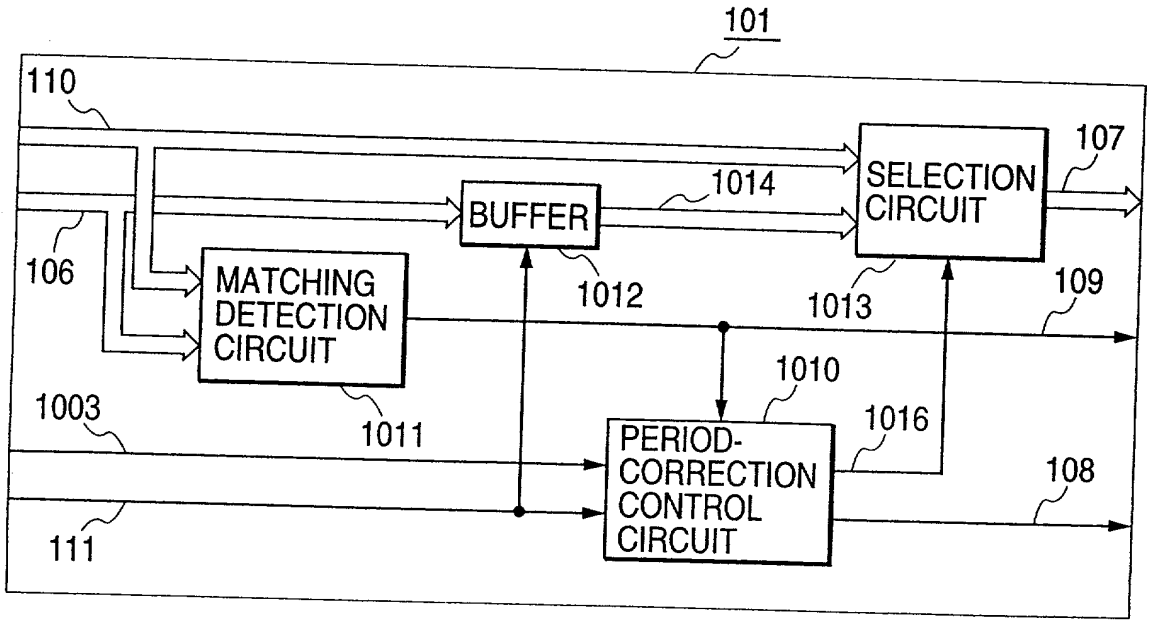

101
110
107
SELECTION
CIRCUIT
1014
BUFFER
106
MATCHING
DETECTION
CIRCUIT
1012
1013
109
1010
1003
1011
1016
PERIOD-
CORRECTION
CONTROL
CIRCUIT
108
111

FIG. 8

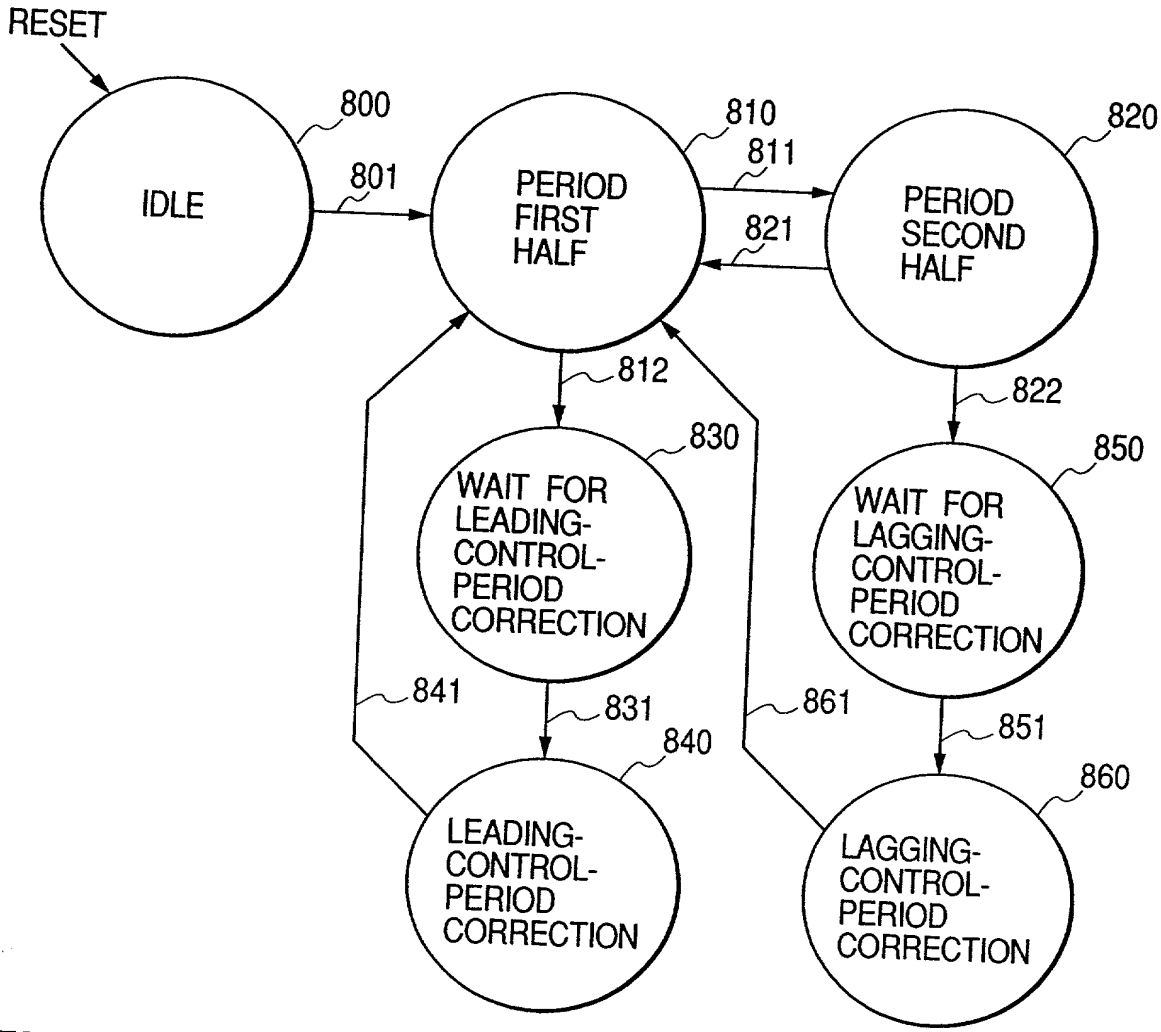

RESET
IDLE
800
801
PERIOD FIRST HALF
810
811
821
PERIOD SECOND HALF
820
812
822
WAIT FOR LEADING-CONTROL-PERIOD CORRECTION
830
WAIT FOR LAGGING-CONTROL-PERIOD CORRECTION
850
841
831
861
851
LEADING-CONTROL-PERIOD CORRECTION
840
LAGGING-CONTROL-PERIOD CORRECTION
860

FIG. 9

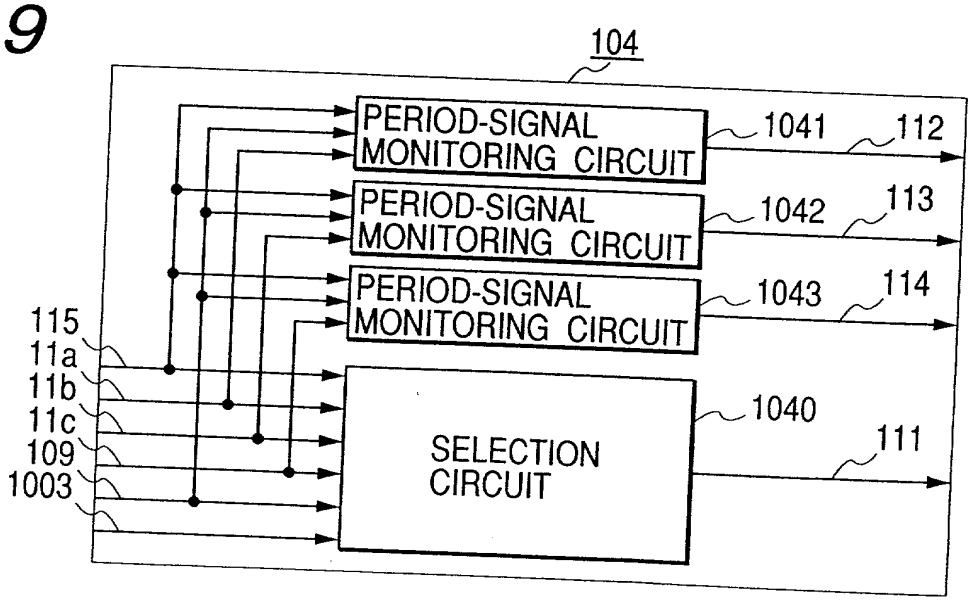

104
PERIOD-SIGNAL MONITORING CIRCUIT
1041
112
PERIOD-SIGNAL MONITORING CIRCUIT
1042
113
PERIOD-SIGNAL MONITORING CIRCUIT
1043
114
115
11a
11b
11c
109
1003
SELECTION CIRCUIT
1040
111

FIG. 10

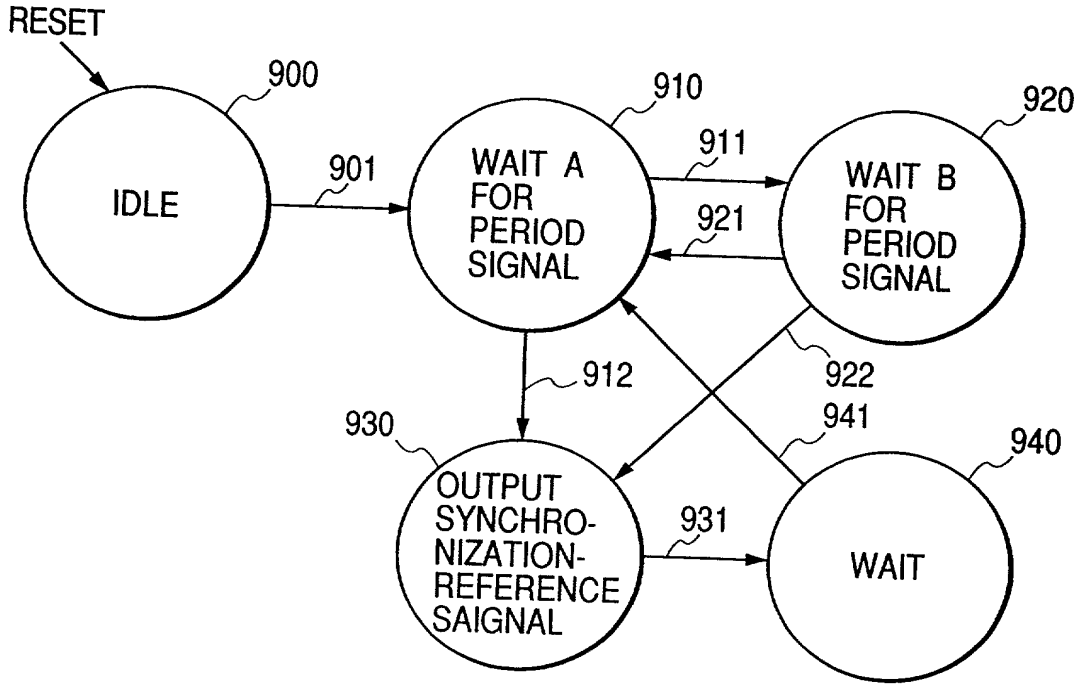

RESET
900
IDLE
901
910
WAIT A FOR PERIOD SIGNAL
911
921
920
WAIT B FOR PERIOD SIGNAL
912
922
930
941
940
OUTPUT SYNCHRO-NIZATION-REFERENCE SAIGNAL
931
WAIT

FIG. 11

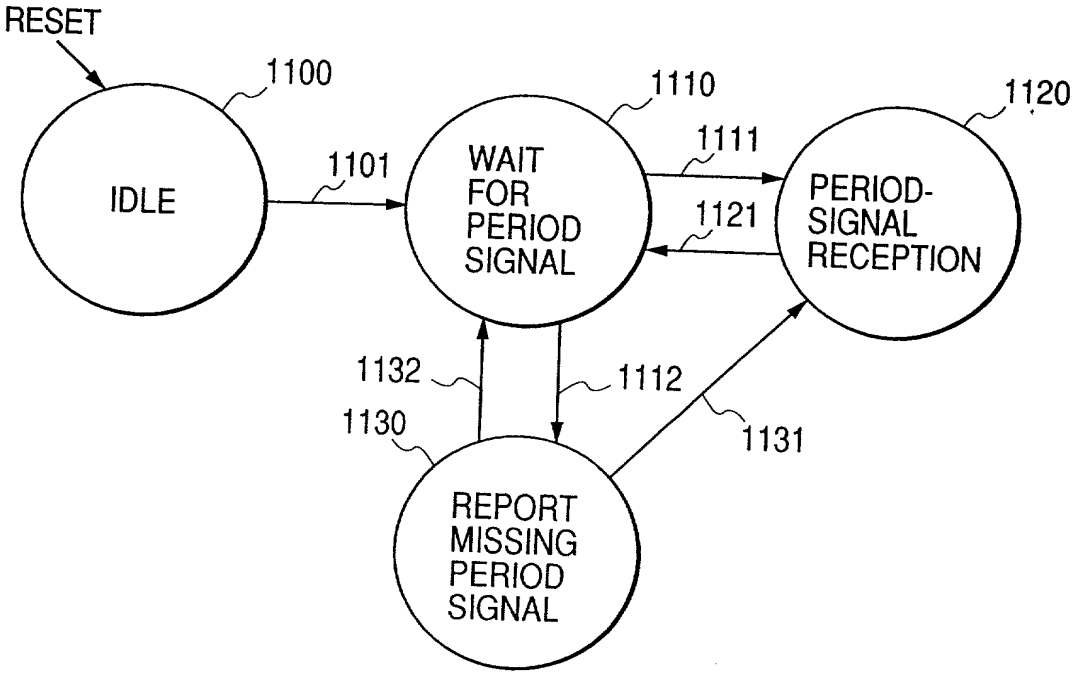

RESET
1100
IDLE
1101
1110
WAIT FOR PERIOD SIGNAL
1111
1121
1120
PERIOD-SIGNAL RECEPTION
1132
1112
1130
1131
REPORT MISSING PERIOD SIGNAL

FIG. 12

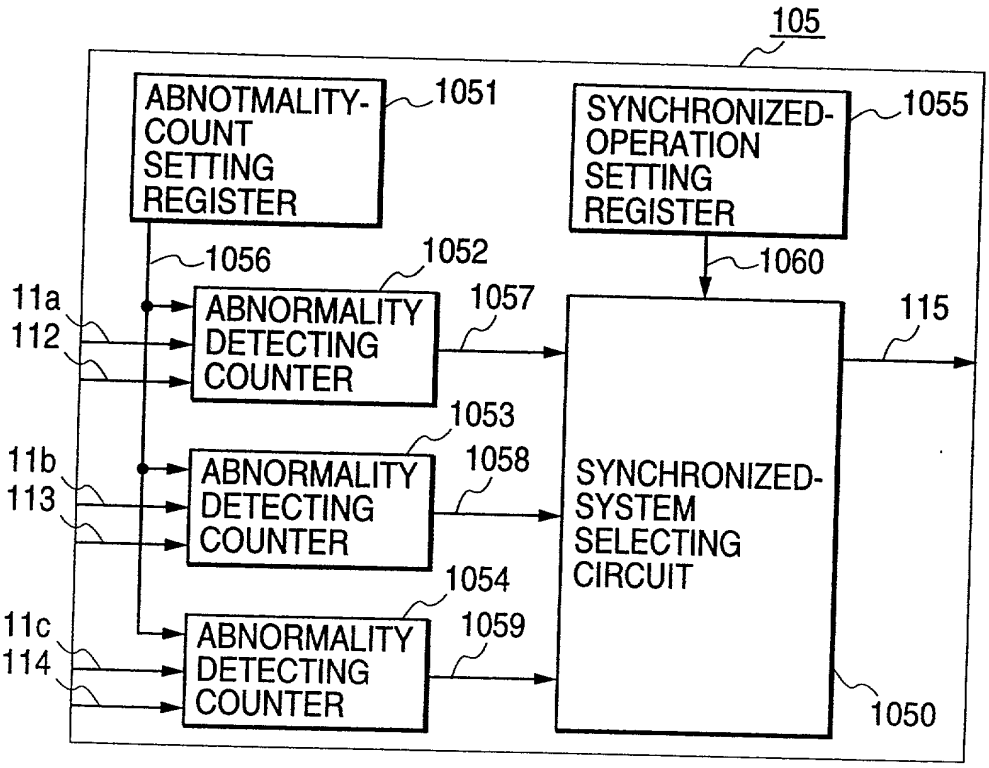

105
ABNOTMALITY-COUNT SETTING REGISTER
1051
SYNCHRONIZED-OPERATION SETTING REGISTER
1055
1056
1052
1060
11a
112
ABNORMALITY DETECTING COUNTER
1057
115
1053
11b
113
ABNORMALITY DETECTING COUNTER
1058
SYNCHRONIZED-SYSTEM SELECTING CIRCUIT
1054
11c
114
ABNORMALITY DETECTING COUNTER
1059
1050

FIG. 13

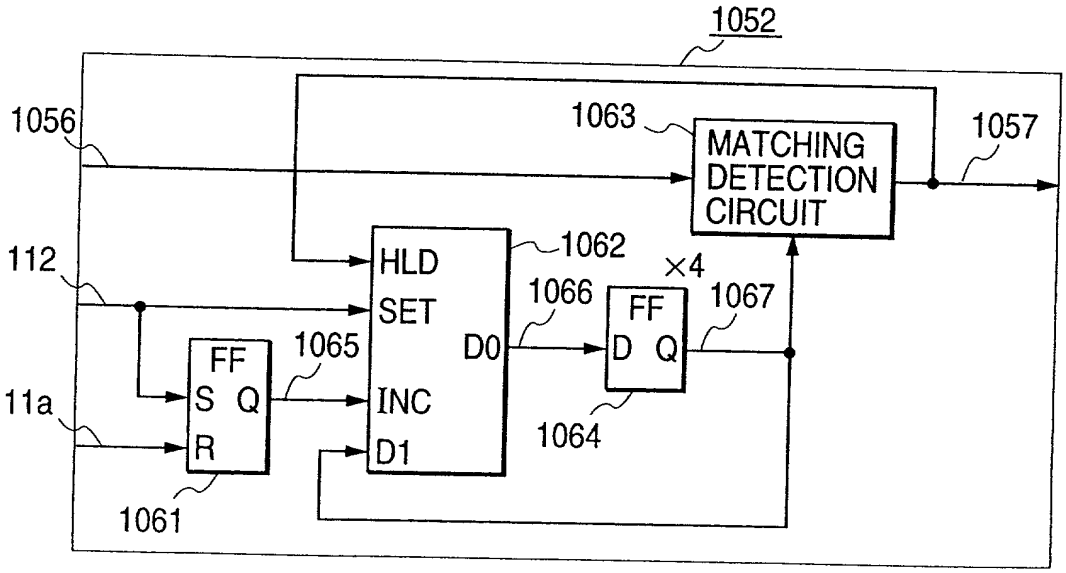

1052
1056
1063
MATCHING DETECTION CIRCUIT
1057
112
HLD
SET
INC
D1
D0
1062
×4
1066
FF
D Q
1067
1065
FF
S Q
R
11a
1064
1061

FIG. 14

SET	INC	HLD	DO
0	0	0	DI
0	0	1	DI
0	1	0	DI
0	1	1	DI
1	0	0	1
1	0	1	DI
1	1	0	DI+1
1	1	1	DI

FIG. 15

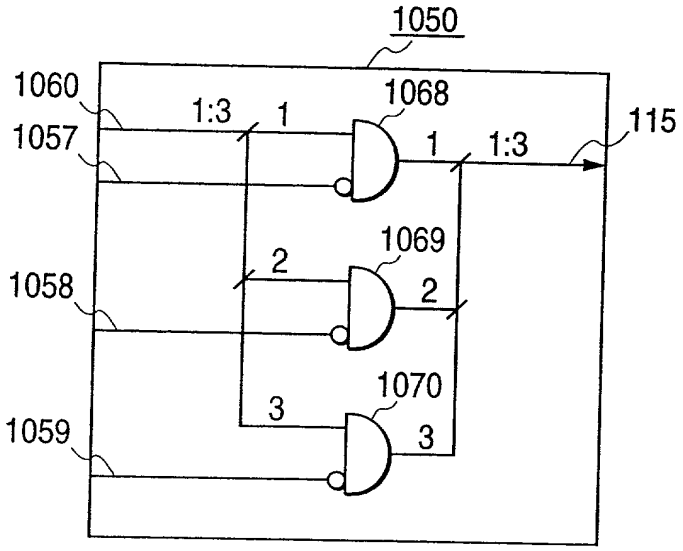


FIG. 16

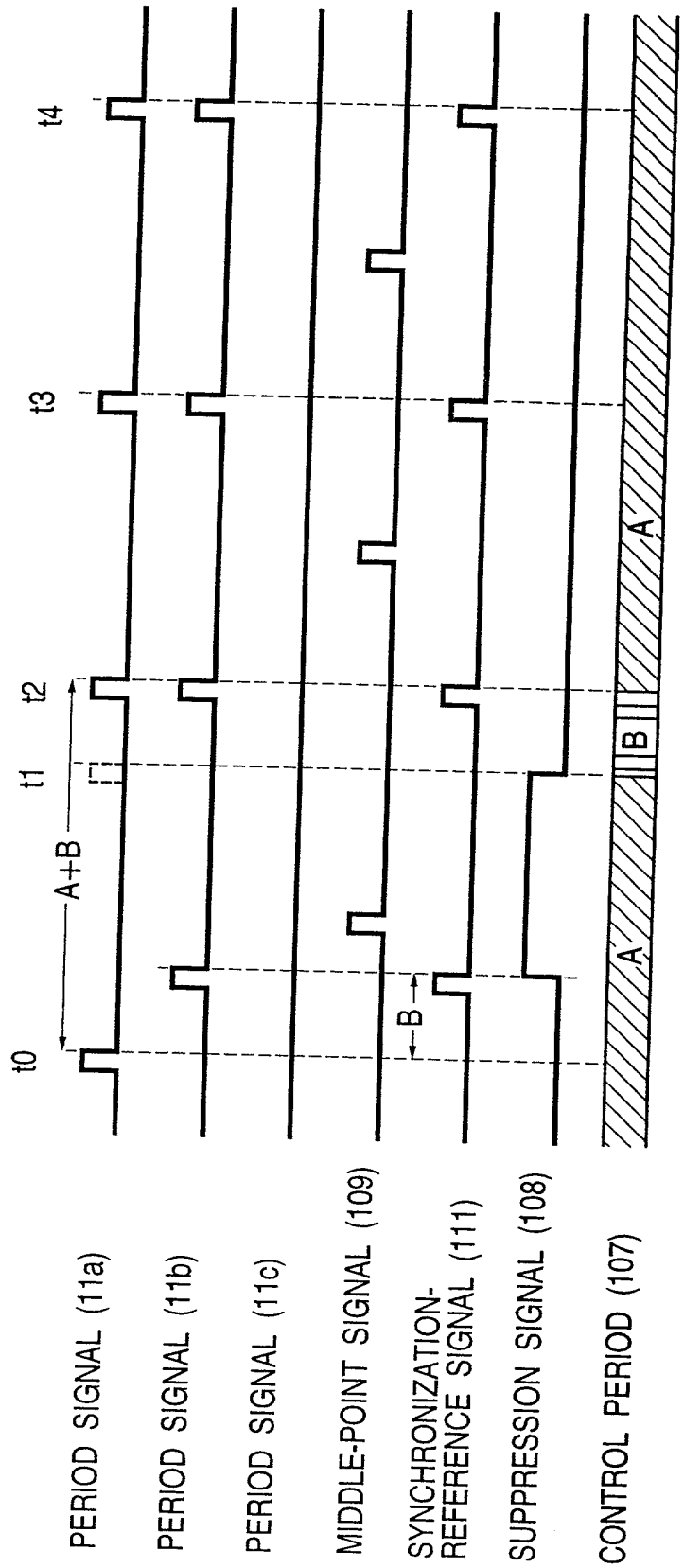

t0
t1
t2
t3
t4
A+B
B
A
B
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (109)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)

FIG. 17

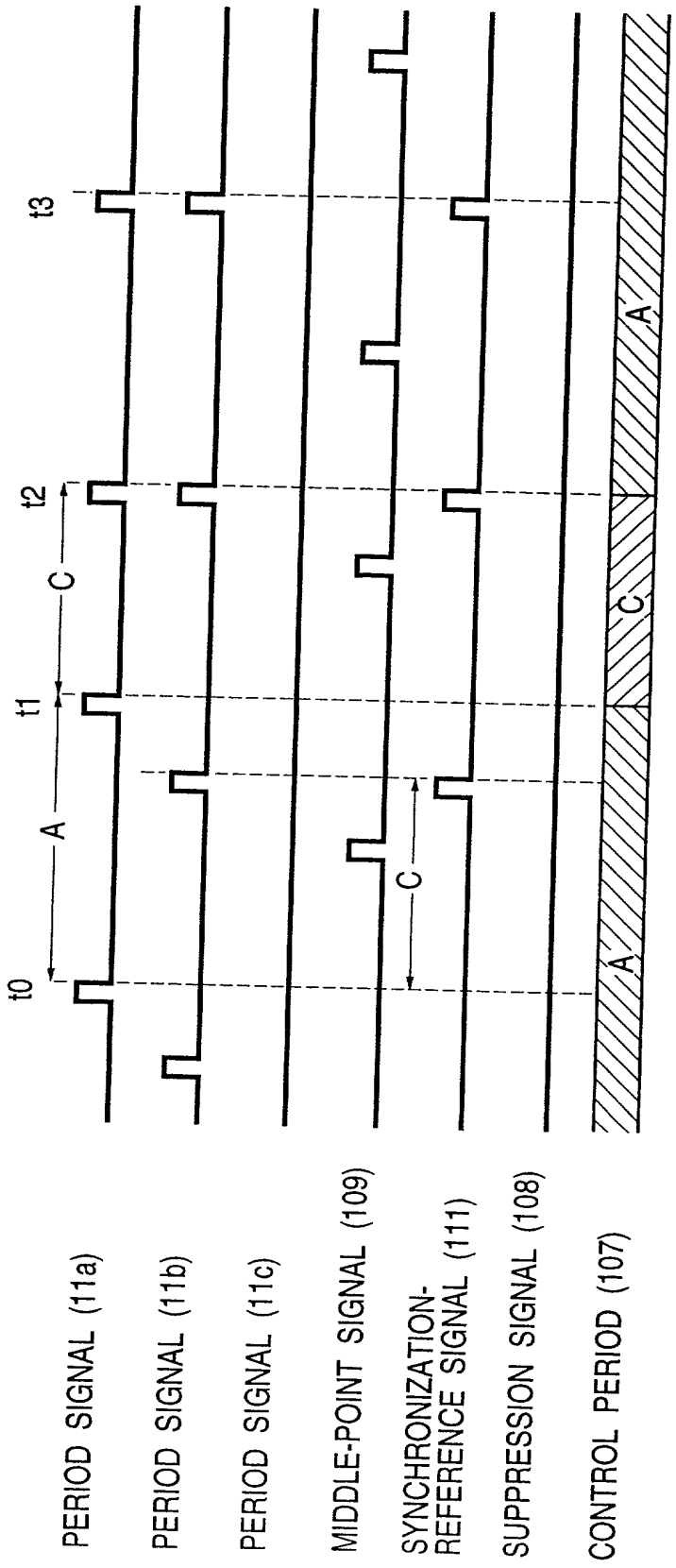

t0
t1
t2
t3
A
C
C
A
C
A
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (109)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)

FIG. 18

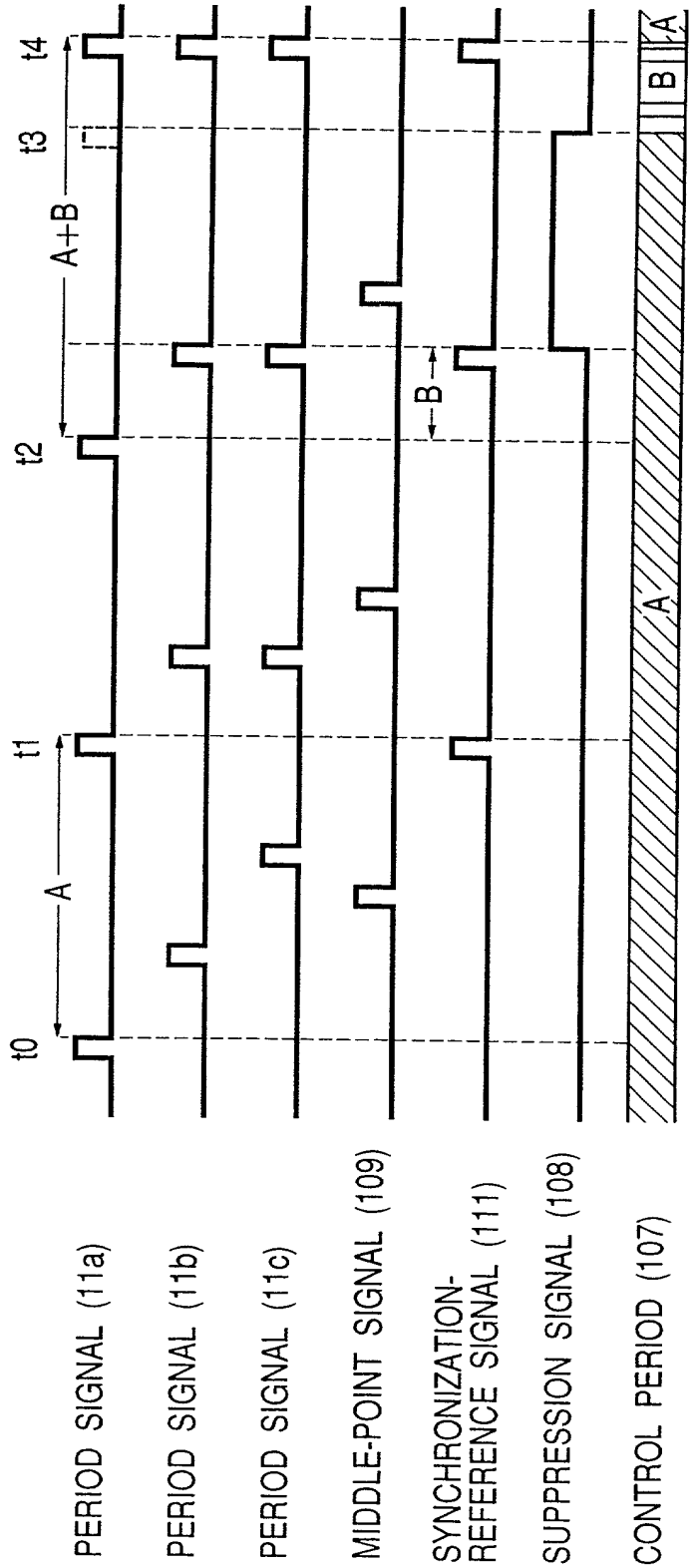

t0
t1
t2
t3
t4
A
A+B
B
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (109)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)
A
B
A

FIG. 19

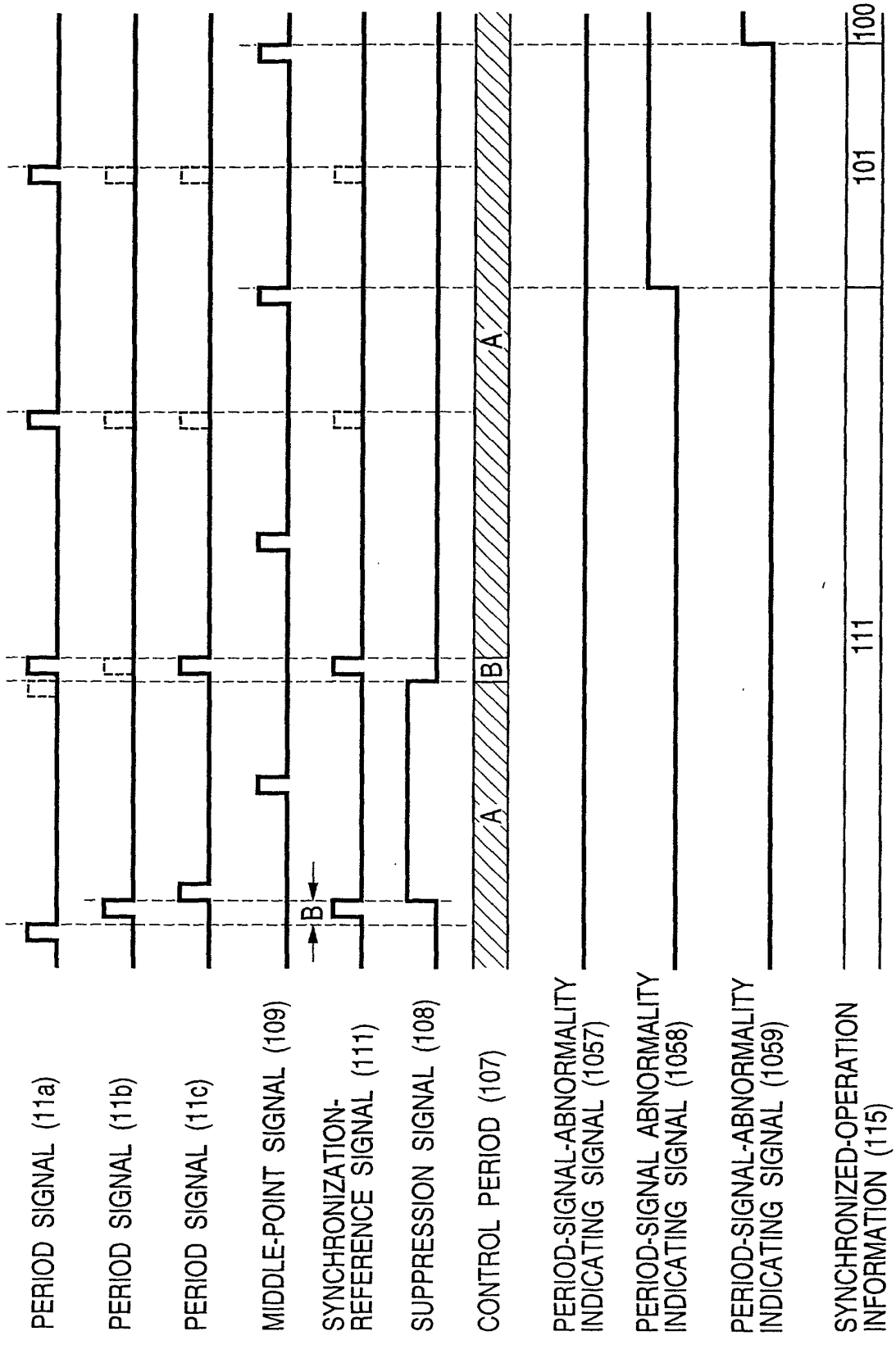

t0
t1 t2
t3
t4
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (109)
B
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)
A
B
A
PERIOD-SIGNAL-ABNORMALITY INDICATING SIGNAL (1057)
PERIOD-SIGNAL ABNORMALITY INDICATING SIGNAL (1058)
PERIOD-SIGNAL-ABNORMALITY INDICATING SIGNAL (1059)
SYNCHRONIZED-OPERATION INFORMATION (115)
111
101
100

FIG. 20

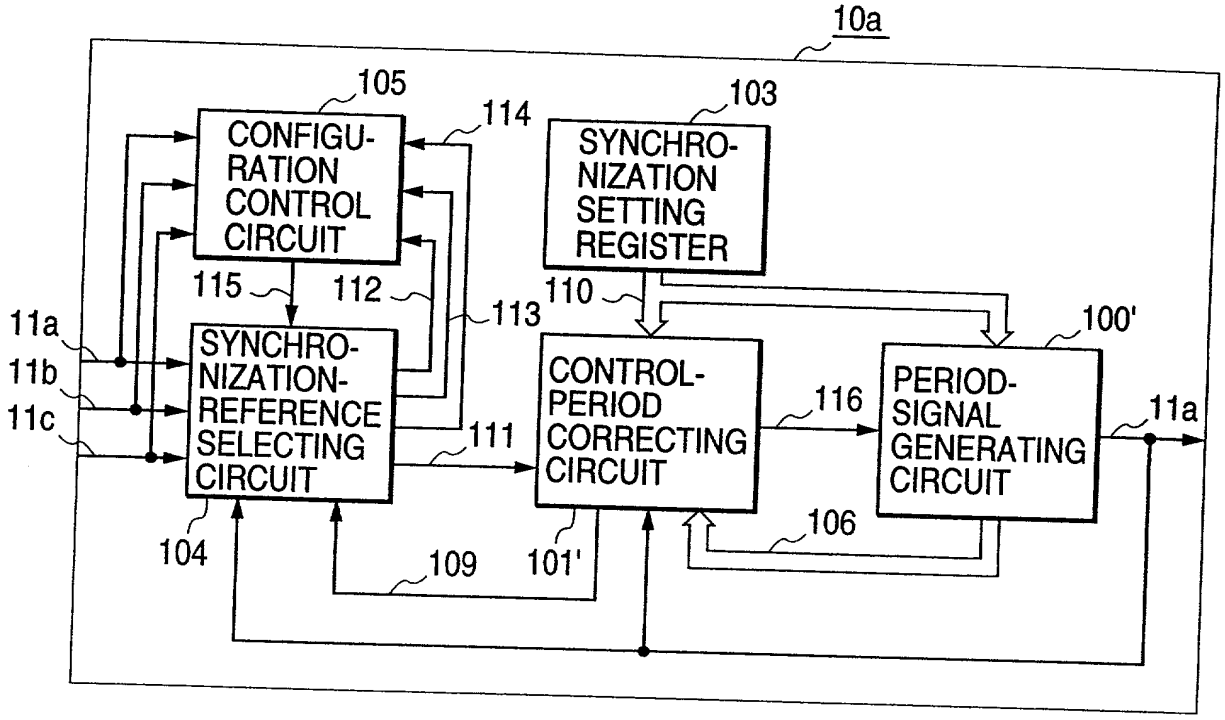

10a
105
CONFIGU-
RATION
CONTROL
CIRCUIT
114
103
SYNCHRO-
NIZATION
SETTING
REGISTER
115
112
113
110
100'
11a
11b
11c
SYNCHRO-
NIZATION-
REFERENCE
SELECTING
CIRCUIT
CONTROL-
PERIOD
CORRECTING
CIRCUIT
116
PERIOD-
SIGNAL
GENERATING
CIRCUIT
11a
111
106
104
109
101'

FIG. 21

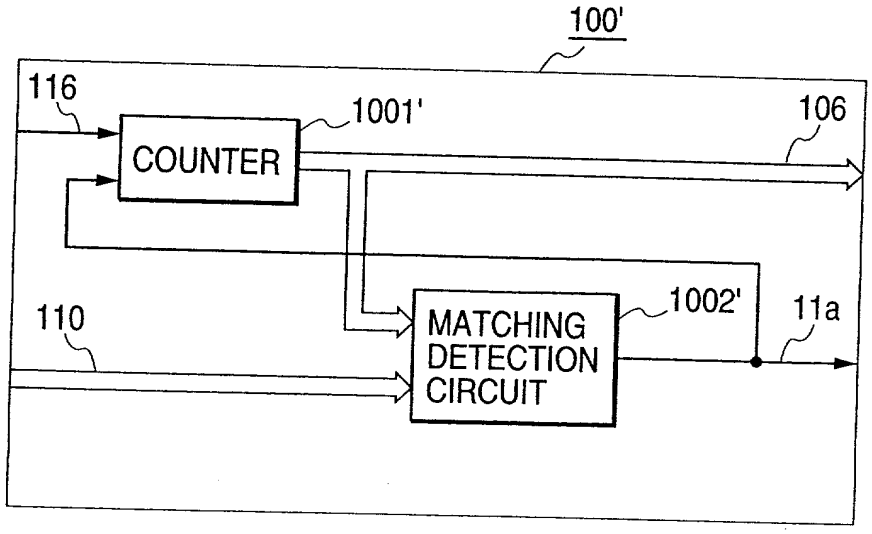

100'
116
1001'
106
COUNTER
110
MATCHING
DETECTION
CIRCUIT
1002'
11a

FIG. 22

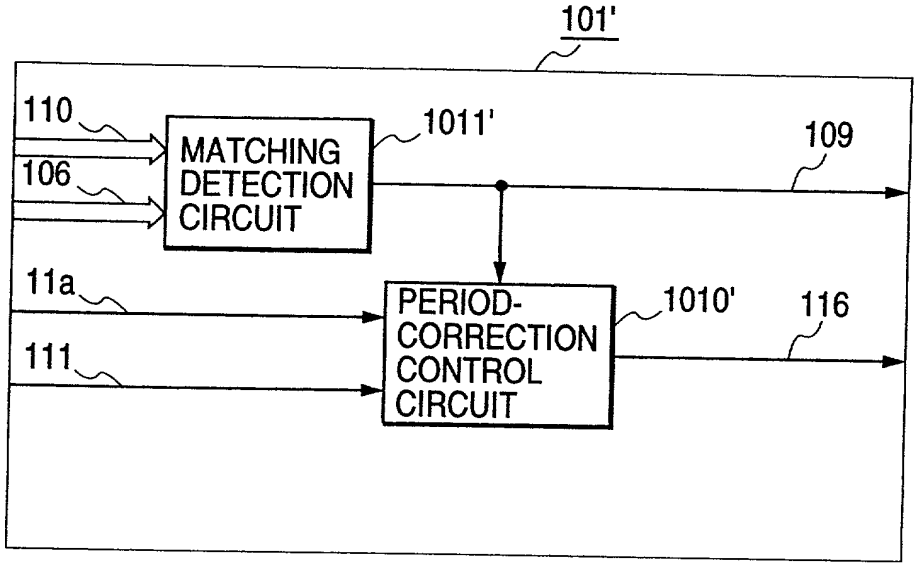

101'
110
106
MATCHING DETECTION CIRCUIT
1011'
109
11a
111
PERIOD-CORRECTION CONTROL CIRCUIT
1010'
116

FIG. 23

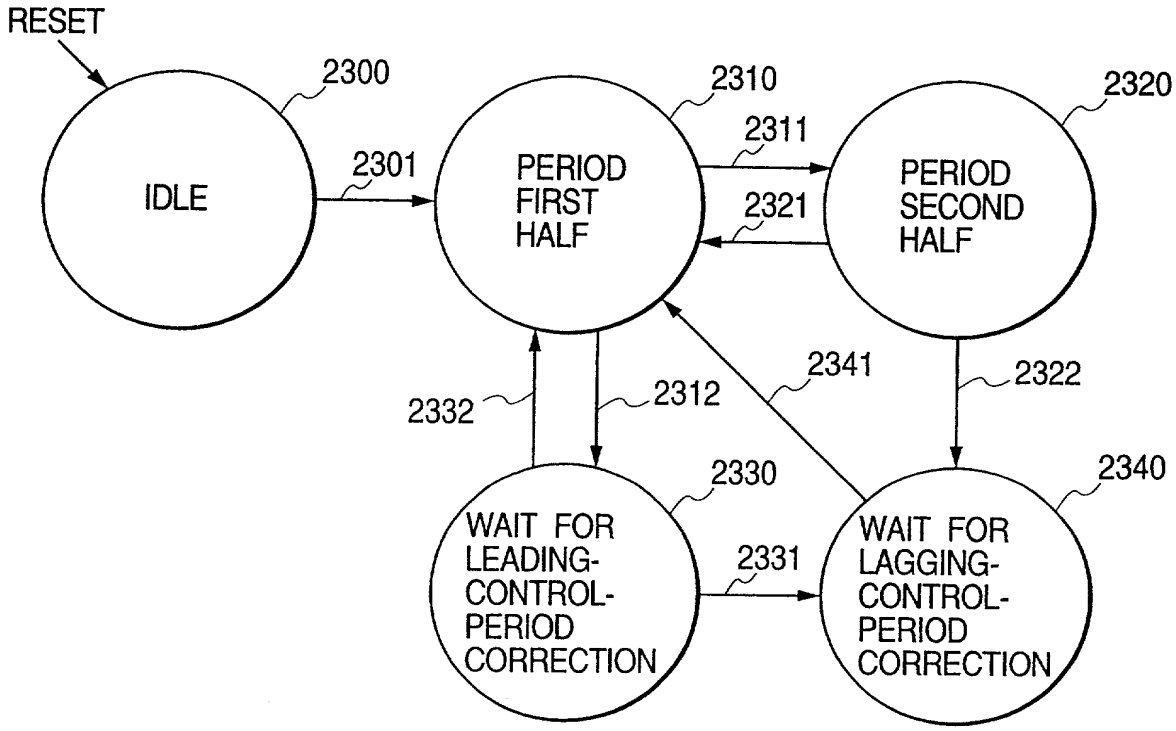

RESET
2300
IDLE
2301
2310
PERIOD FIRST HALF
2311
2321
2320
PERIOD SECOND HALF
2332
2312
2341
2322
2330
WAIT FOR LEADING-CONTROL-PERIOD CORRECTION
2331
2340
WAIT FOR LAGGING-CONTROL-PERIOD CORRECTION

FIG. 24

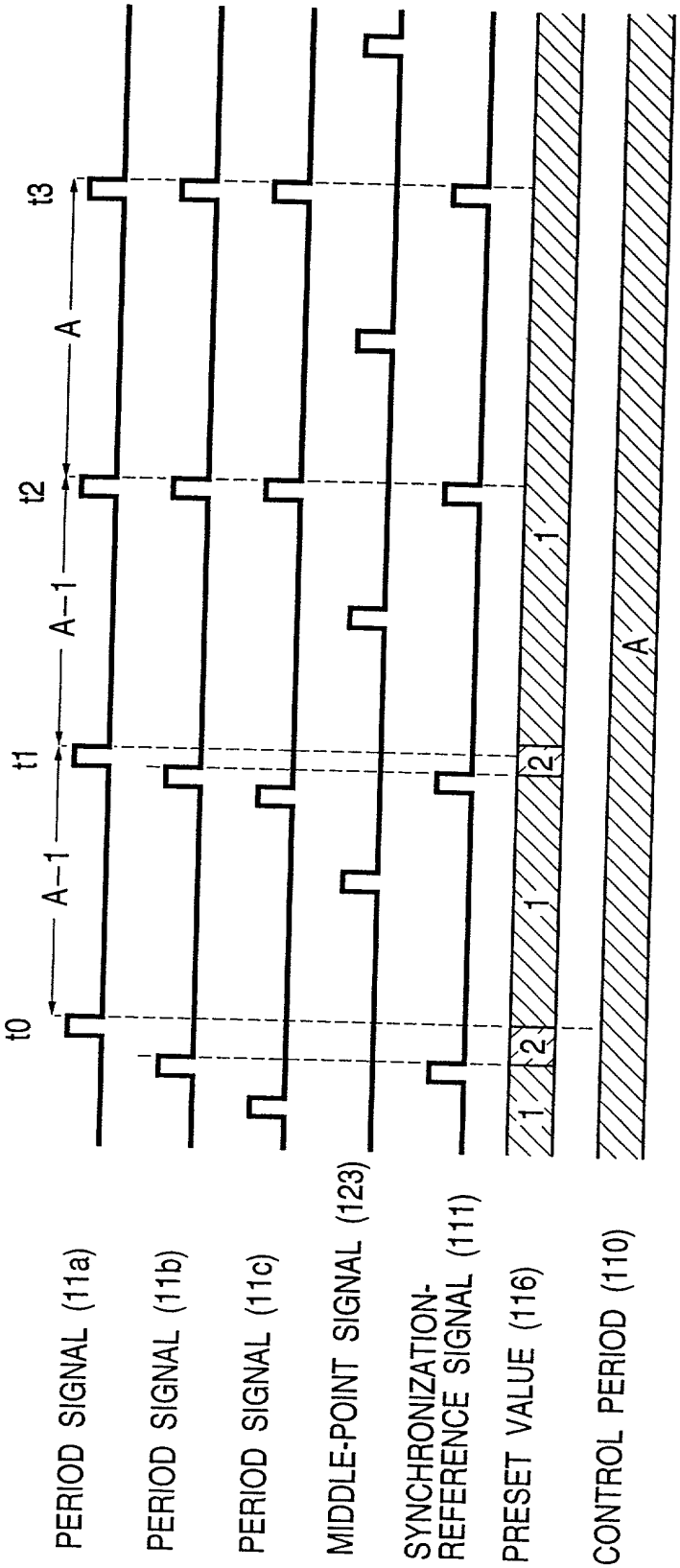

t0
t1
t2
t3
A−1
A−1
A
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (123)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
PRESET VALUE (116)
CONTROL PERIOD (110)
1
2
1
2
1
2
A

FIG. 25

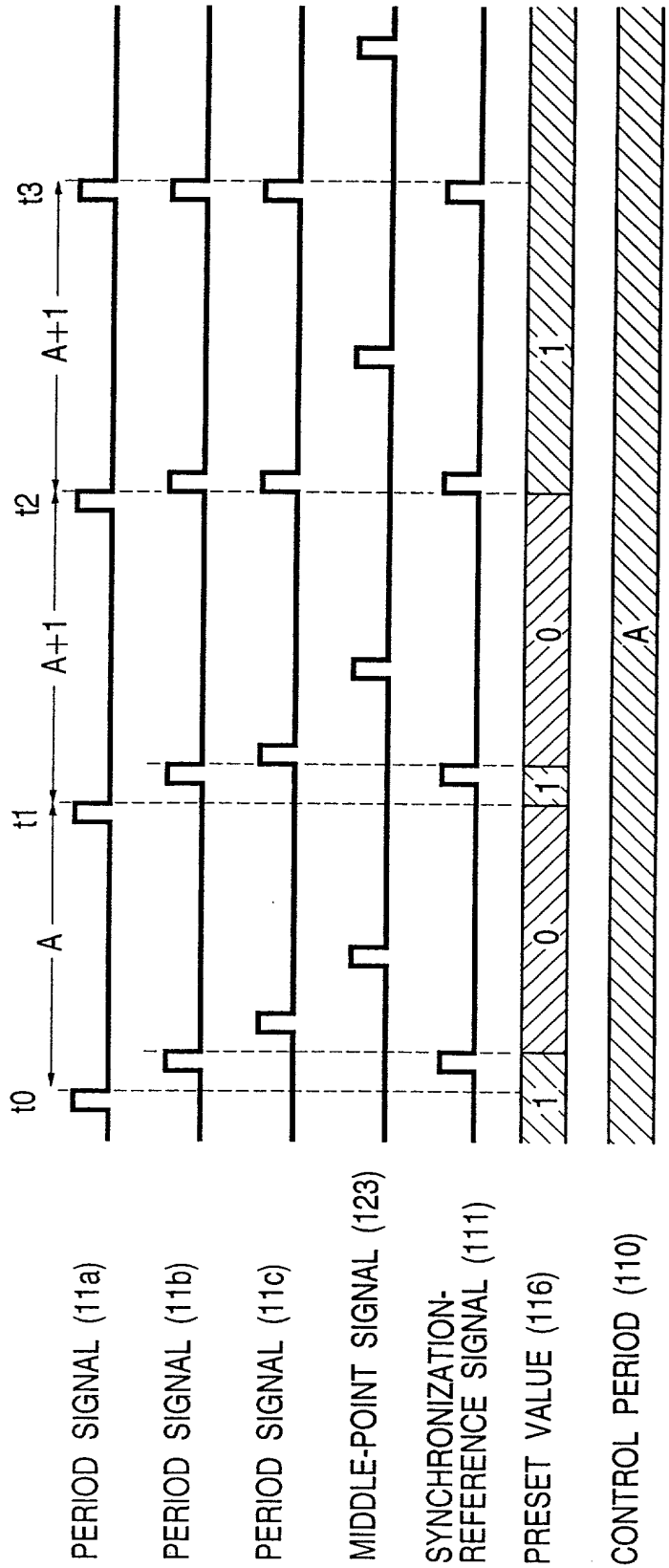

t0
A
t1
A+1
t2
A+1
t3
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (123)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
PRESET VALUE (116)
1
0
1
0
1
CONTROL PERIOD (110)
A

FIG. 26

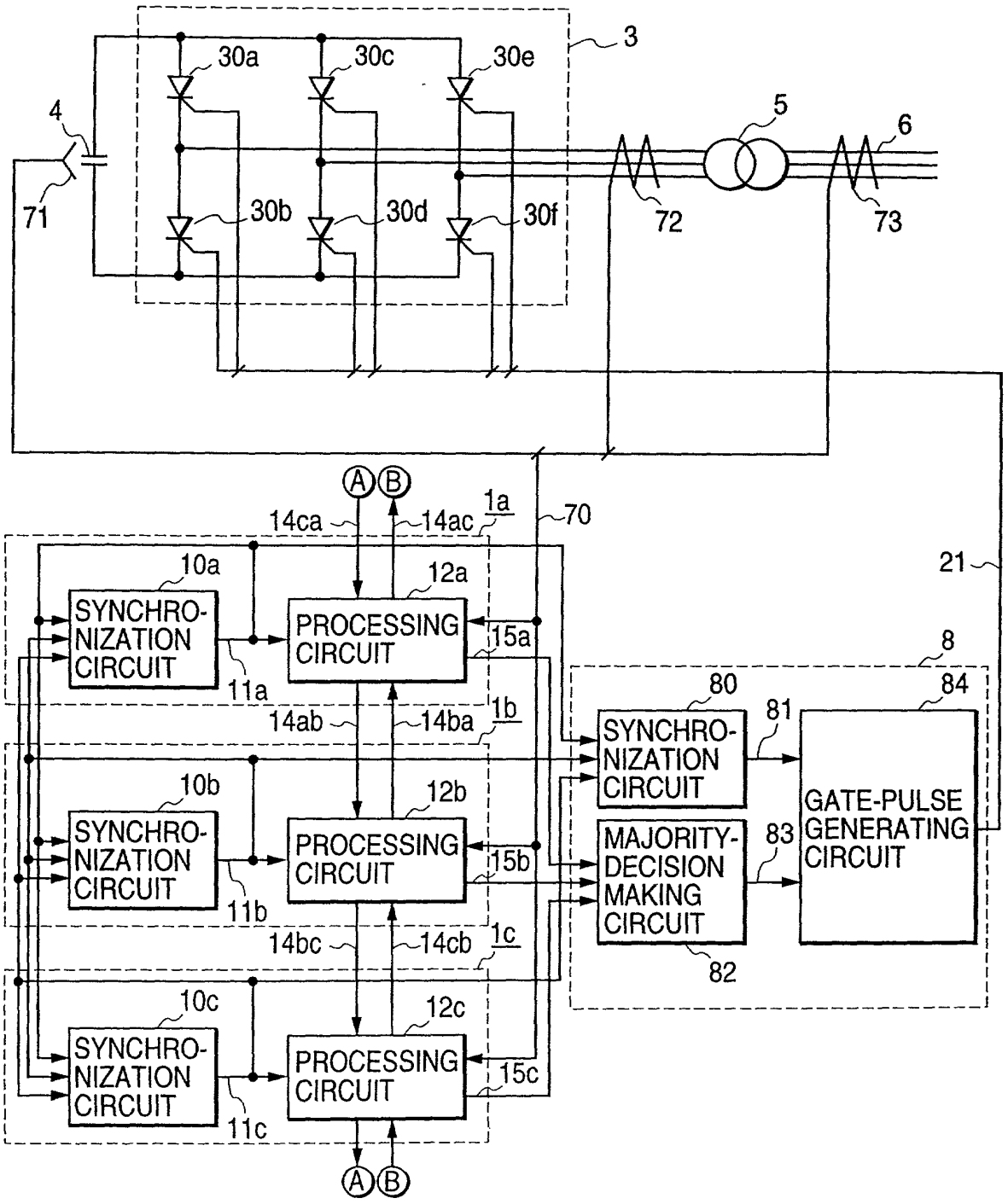

3
30a
30c
30e
4
5
6
71
30b
30d
30f
72
73
A
B
14ca
14ac
1a
70
21
10a
12a
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
15a
11a
8
80
84
14ab
14ba
1b
81
SYNCHRO-NIZATION CIRCUIT
10b
12b
GATE-PULSE GENERATING CIRCUIT
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
15b
MAJORITY-DECISION MAKING CIRCUIT
83
11b
14bc
14cb
1c
82
10c
12c
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
15c
11c
A
B

FIG. 27

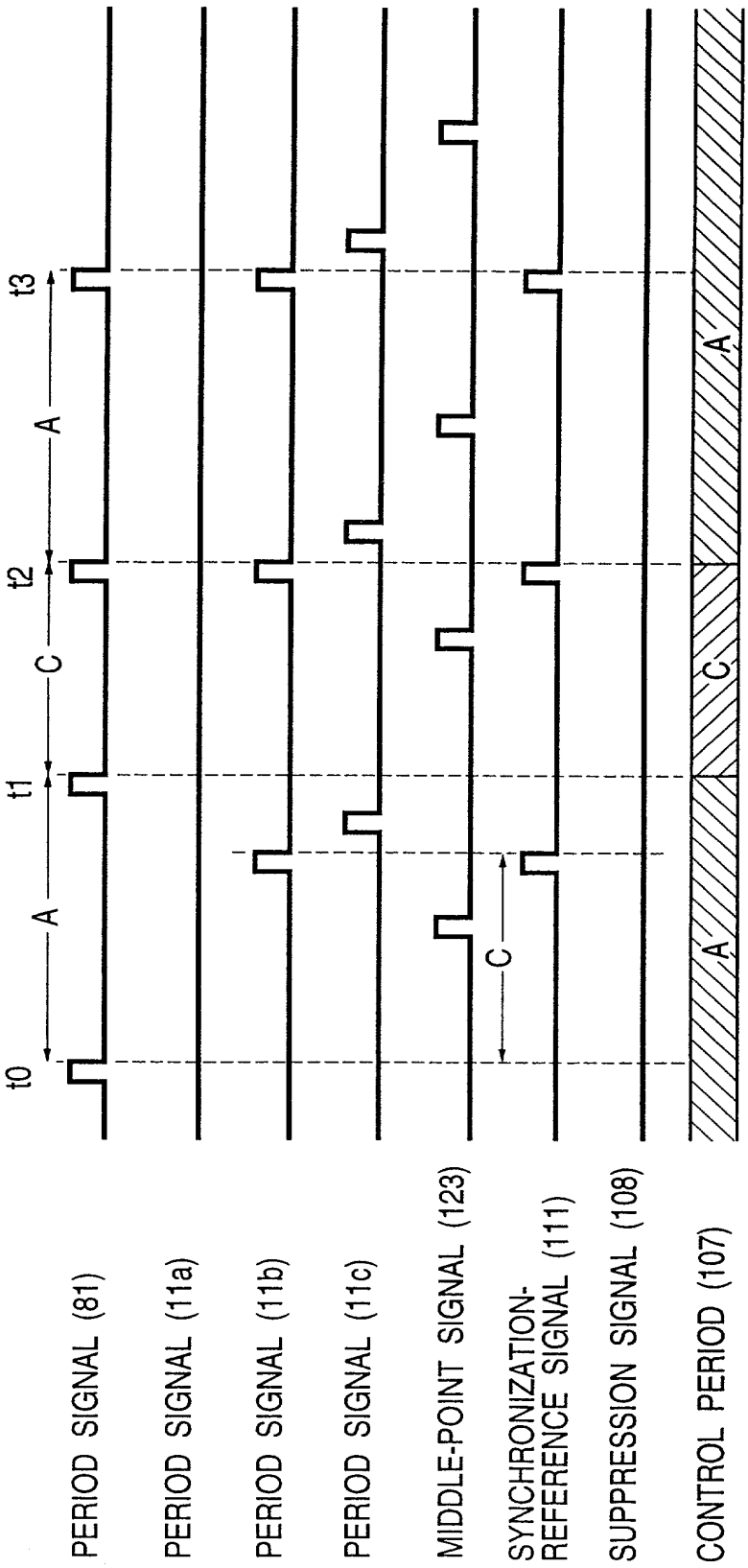

t0
t1
t2
t3
A
C
A
PERIOD SIGNAL (81)
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (123)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)
A
C
A

FIG. 28

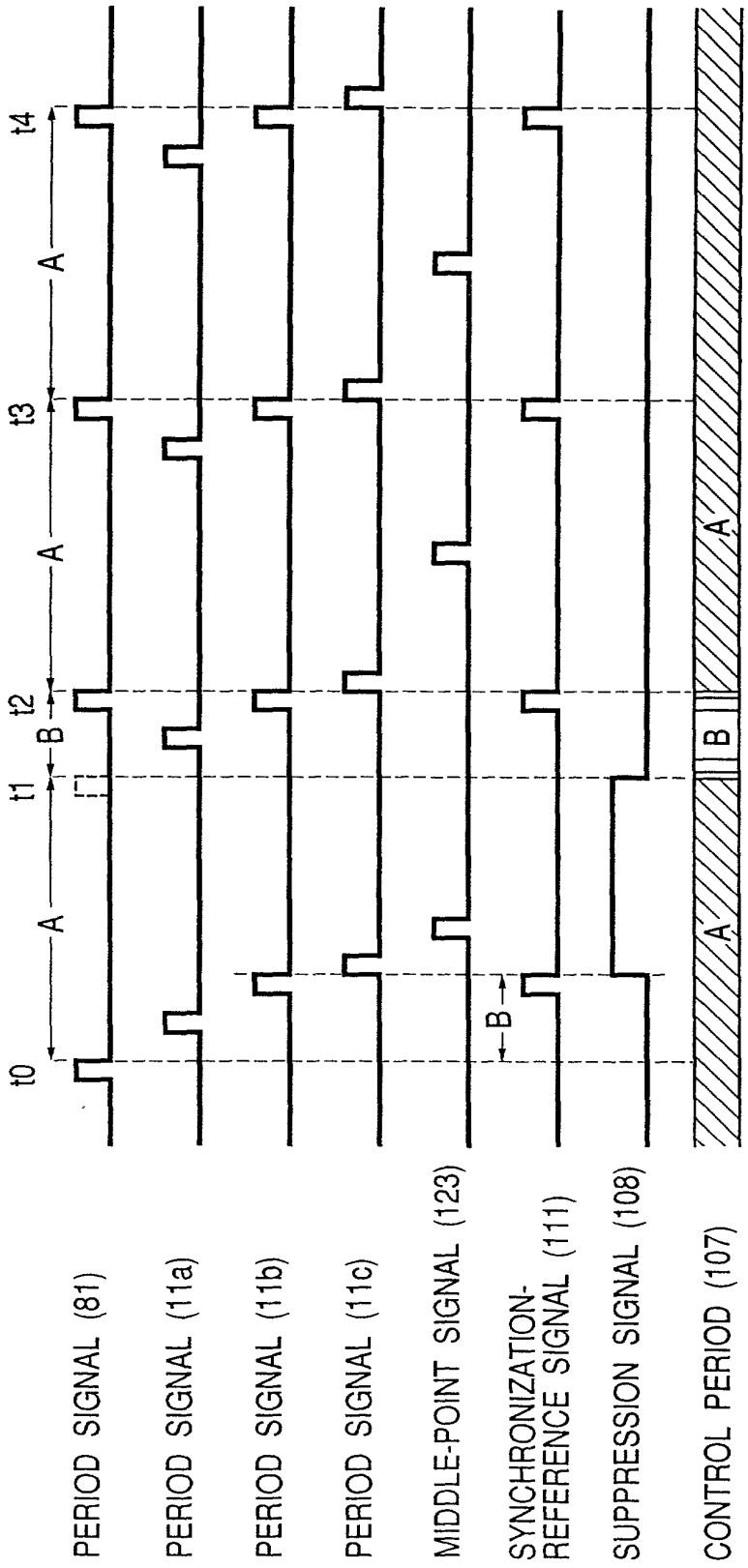

t0
t1
t2
t3
t4
A
B
A
A
B
A
PERIOD SIGNAL (81)
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
MIDDLE-POINT SIGNAL (123)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)

FIG. 29

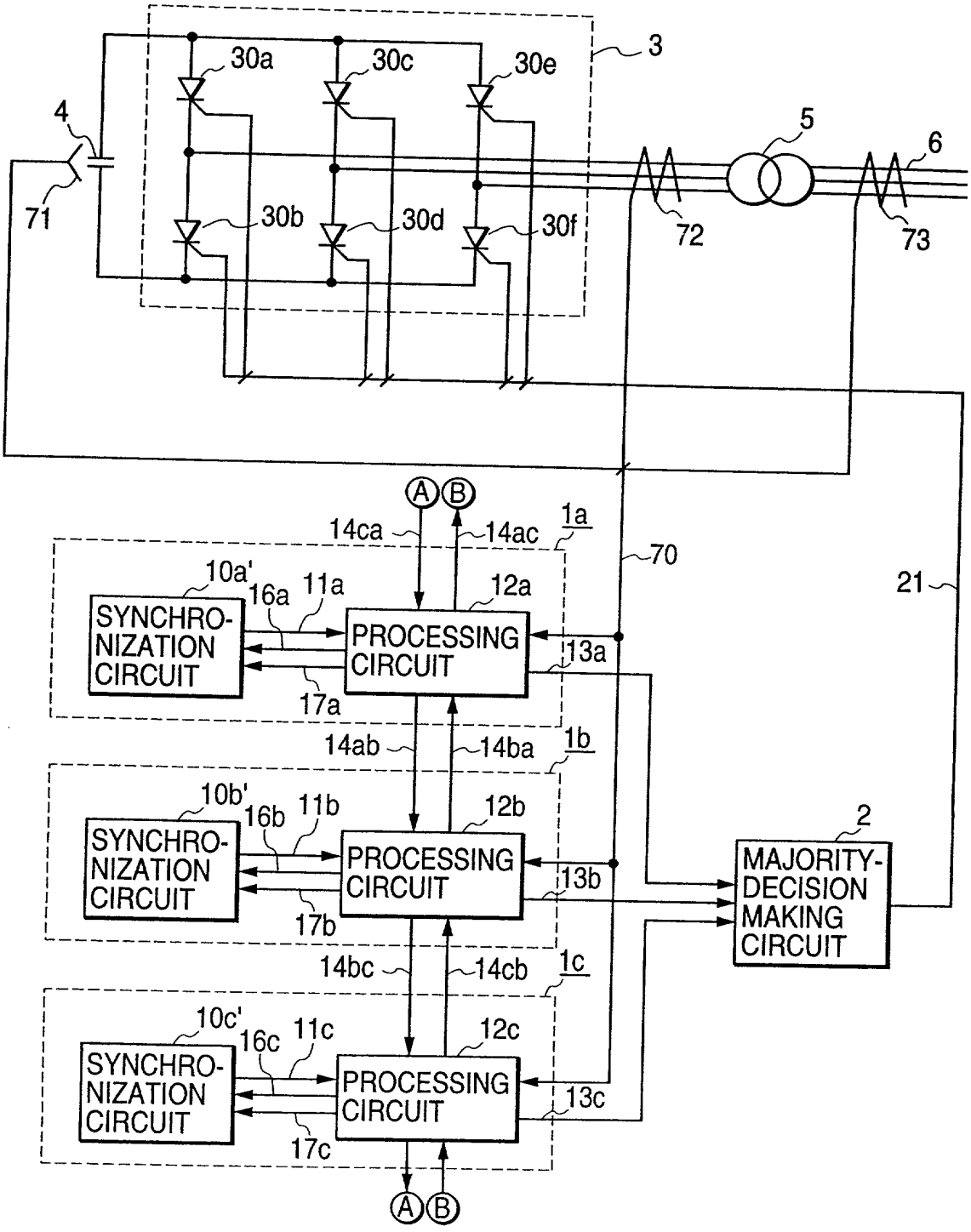

3
30a
30c
30e
4
5
6
71
30b
30d
30f
72
73
A
B
14ca
14ac
1a
70
21
10a'
16a
11a
12a
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13a
17a
14ab
14ba
1b
10b'
16b
11b
12b
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13b
17b
2
MAJORITY-DECISION MAKING CIRCUIT
14bc
14cb
1c
10c'
16c
11c
12c
SYNCHRO-NIZATION CIRCUIT
PROCESSING CIRCUIT
13c
17c
A
B

FIG. 30

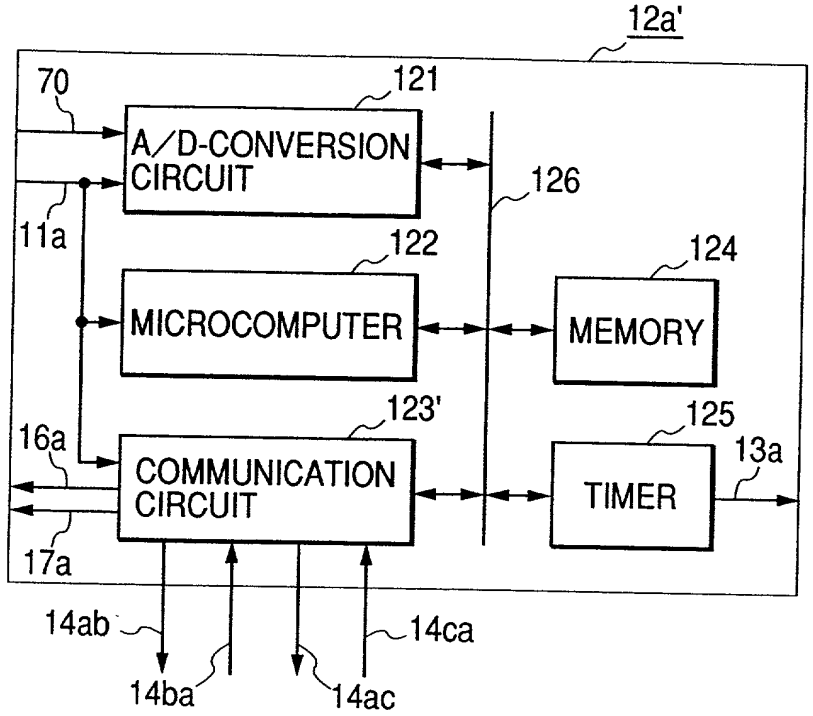

12a'
70
121
A/D-CONVERSION CIRCUIT
126
11a
122
124
MICROCOMPUTER
MEMORY
123'
125
16a
COMMUNICATION CIRCUIT
TIMER
13a
17a
14ab
14ca
14ba
14ac

FIG. 31

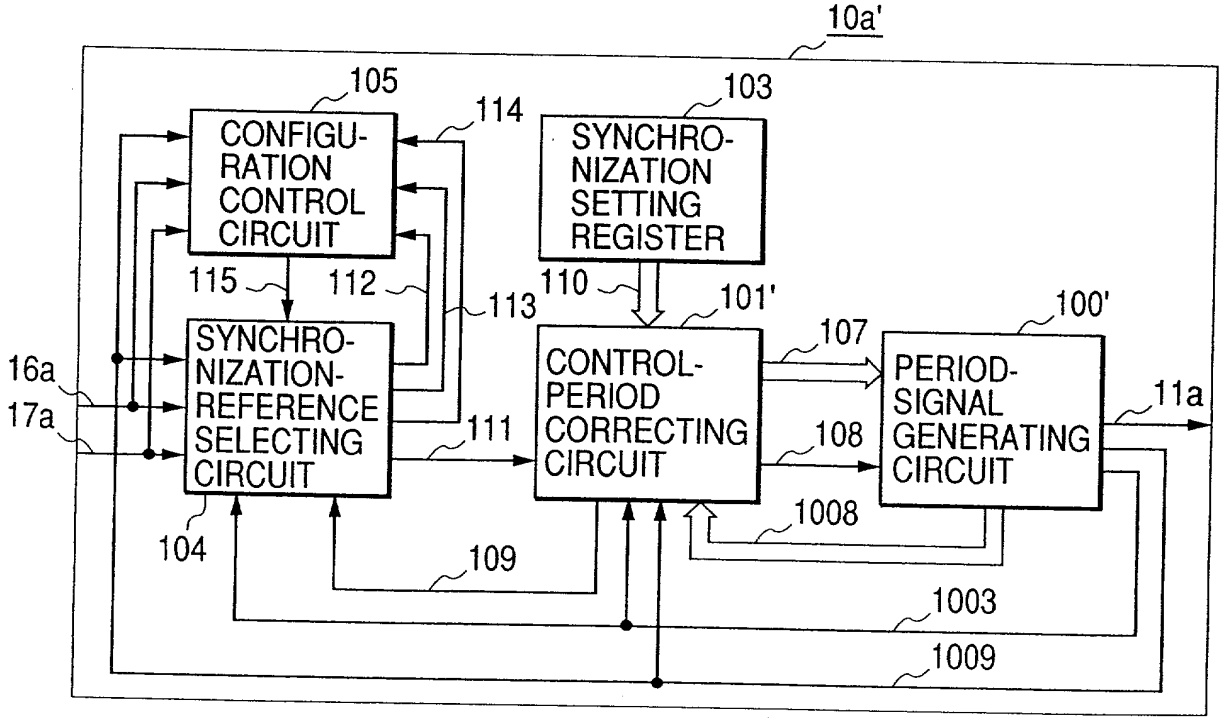

10a'
105
114
103
CONFIGU-RATION CONTROL CIRCUIT
SYNCHRO-NIZATION SETTING REGISTER
115
112
113
110
101'
100'
107
16a
17a
SYNCHRO-NIZATION-REFERENCE SELECTING CIRCUIT
CONTROL-PERIOD CORRECTING CIRCUIT
PERIOD-SIGNAL GENERATING CIRCUIT
11a
111
108
1008
104
109
1003
1009

FIG. 32

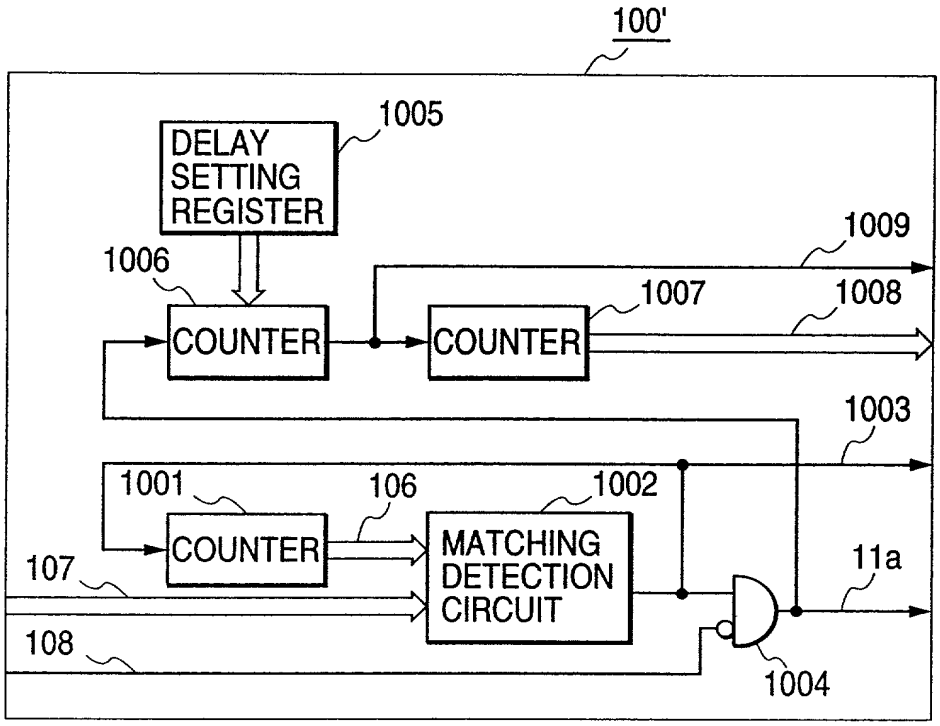

100'
1005
DELAY SETTING REGISTER
1009
1006
1007
1008
COUNTER
COUNTER
1003
1001
106
1002
COUNTER
MATCHING DETECTION CIRCUIT
107
11a
108
1004

FIG. 33

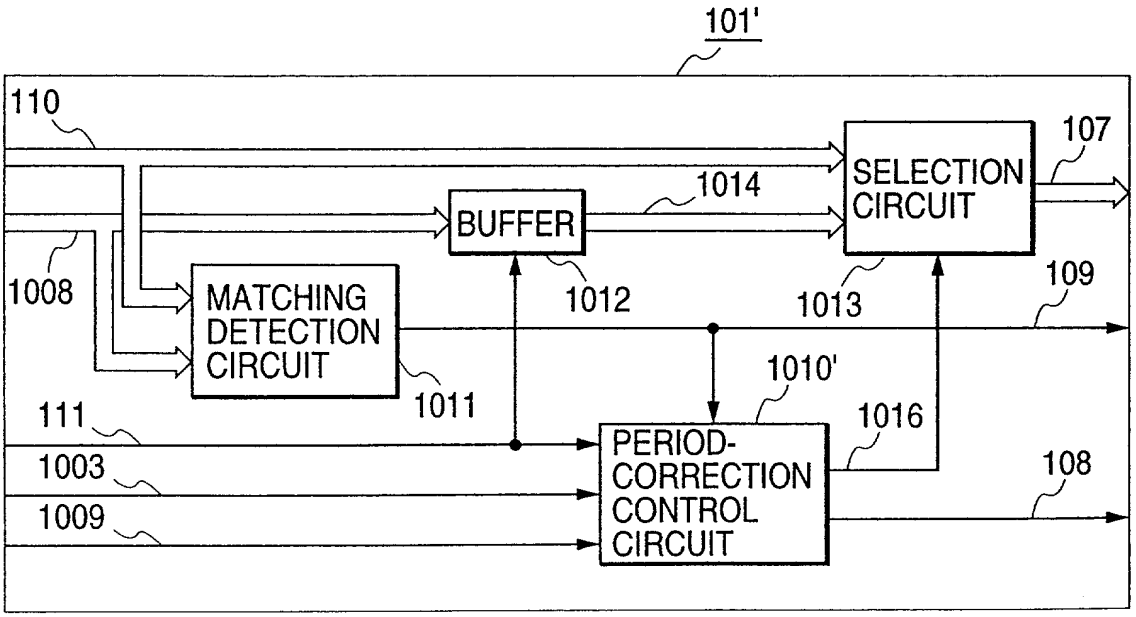

101'
110
107
SELECTION CIRCUIT
1014
BUFFER
1008
1012
1013
109
MATCHING DETECTION CIRCUIT
1010'
1011
1016
111
PERIOD-CORRECTION CONTROL CIRCUIT
108
1003
1009

FIG. 34

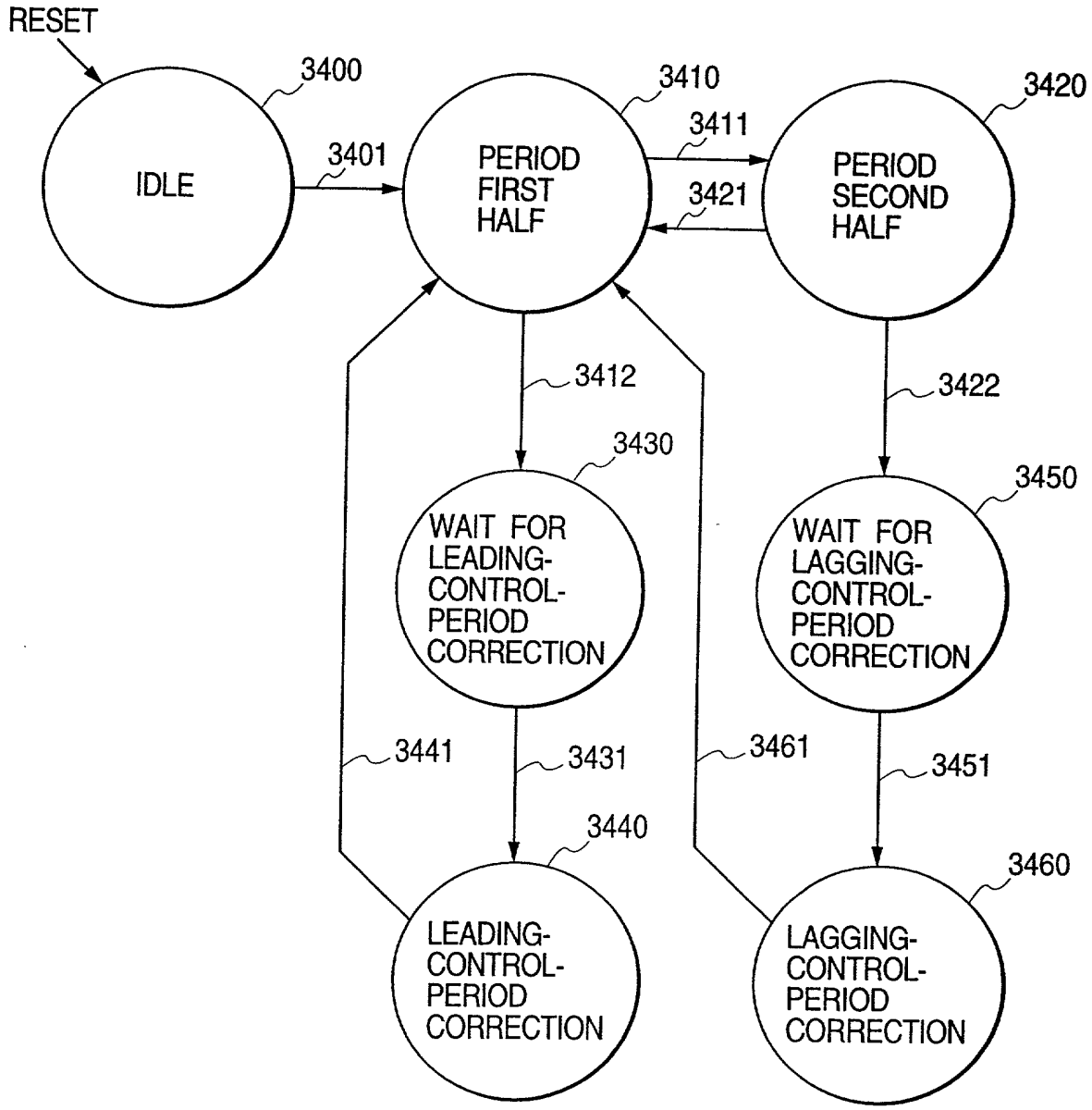

RESET
3400
IDLE
3401
3410
PERIOD FIRST HALF
3411
3421
3420
PERIOD SECOND HALF
3412
3422
3430
WAIT FOR LEADING-CONTROL-PERIOD CORRECTION
3450
WAIT FOR LAGGING-CONTROL-PERIOD CORRECTION
3441
3431
3461
3451
3440
LEADING-CONTROL-PERIOD CORRECTION
3460
LAGGING-CONTROL-PERIOD CORRECTION

FIG. 35

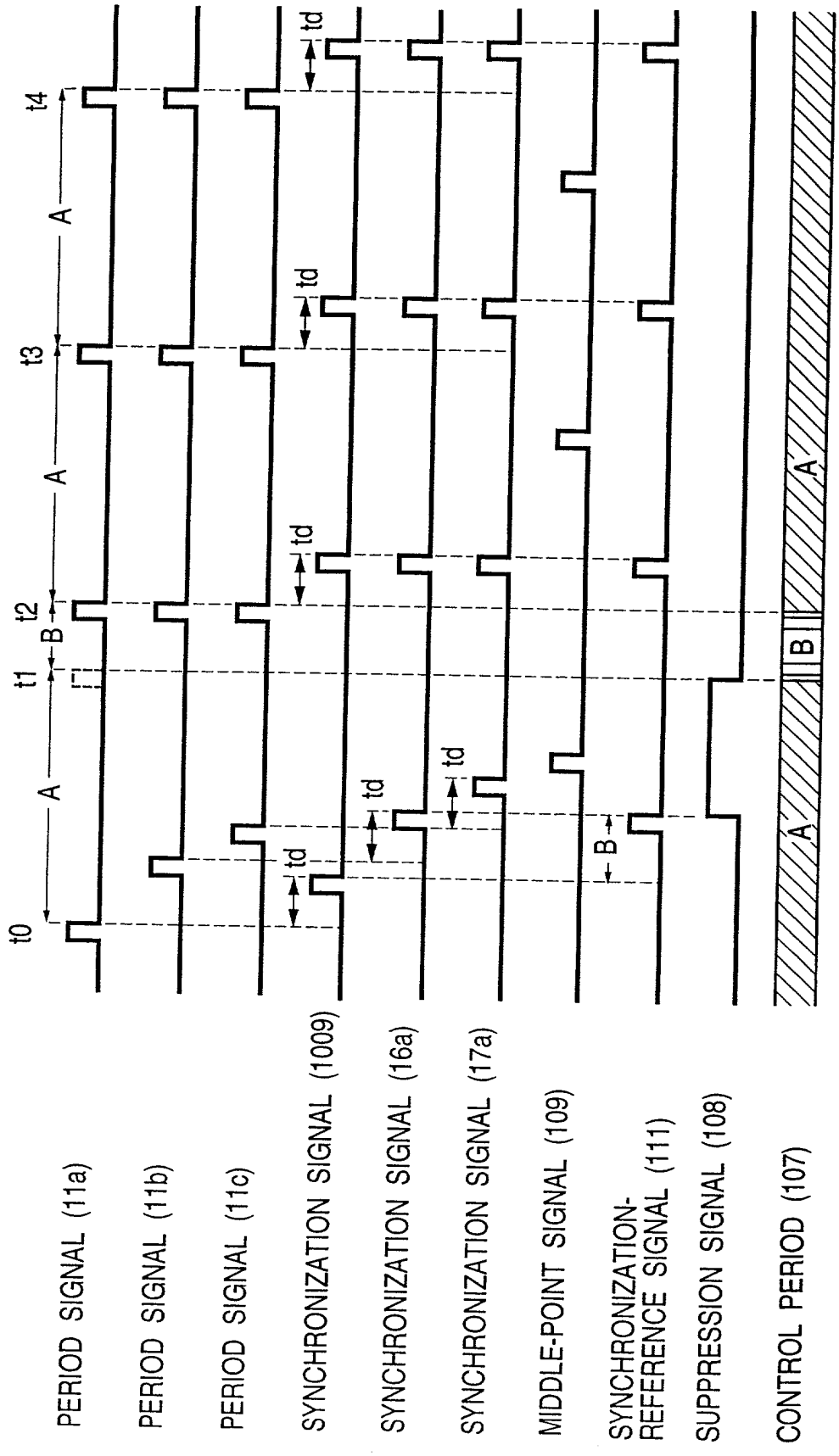

t0
t1
t2
t3
t4
A
B
A
A
td
td
td
td
td
B
A
A
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
SYNCHRONIZATION SIGNAL (1009)
SYNCHRONIZATION SIGNAL (16a)
SYNCHRONIZATION SIGNAL (17a)
MIDDLE-POINT SIGNAL (109)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)

FIG. 36

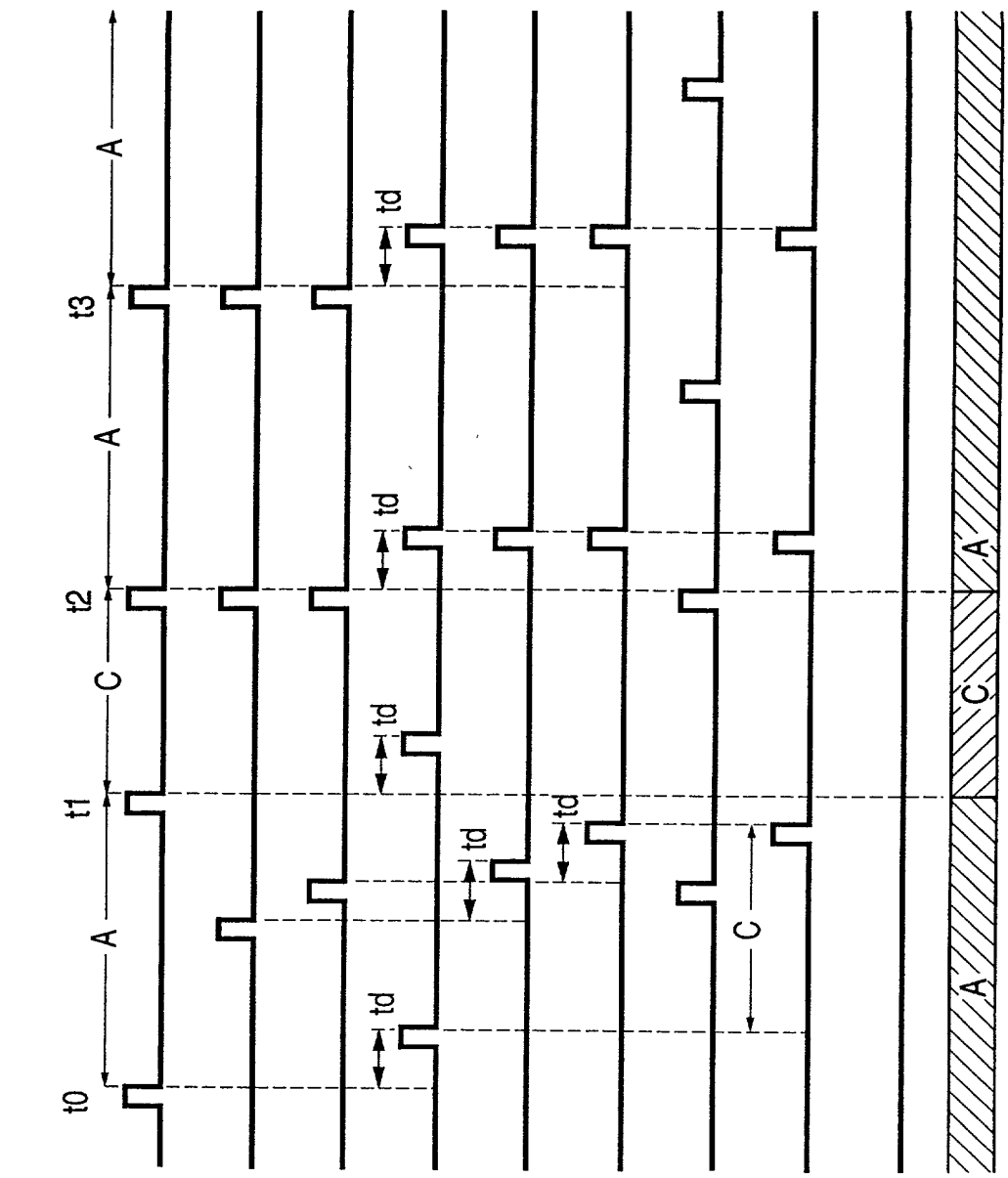

t0
t1
t2
t3
A
C
A
A
td
td
td
td
td
PERIOD SIGNAL (11a)
PERIOD SIGNAL (11b)
PERIOD SIGNAL (11c)
SYNCHRONIZATION SIGNAL (1009)
SYNCHRONIZATION SIGNAL (16a)
SYNCHRONIZATION SIGNAL (17a)
MIDDLE-POINT SIGNAL (109)
SYNCHRONIZATION-REFERENCE SIGNAL (111)
SUPPRESSION SIGNAL (108)
CONTROL PERIOD (107)
A
C
A

FIG. 37

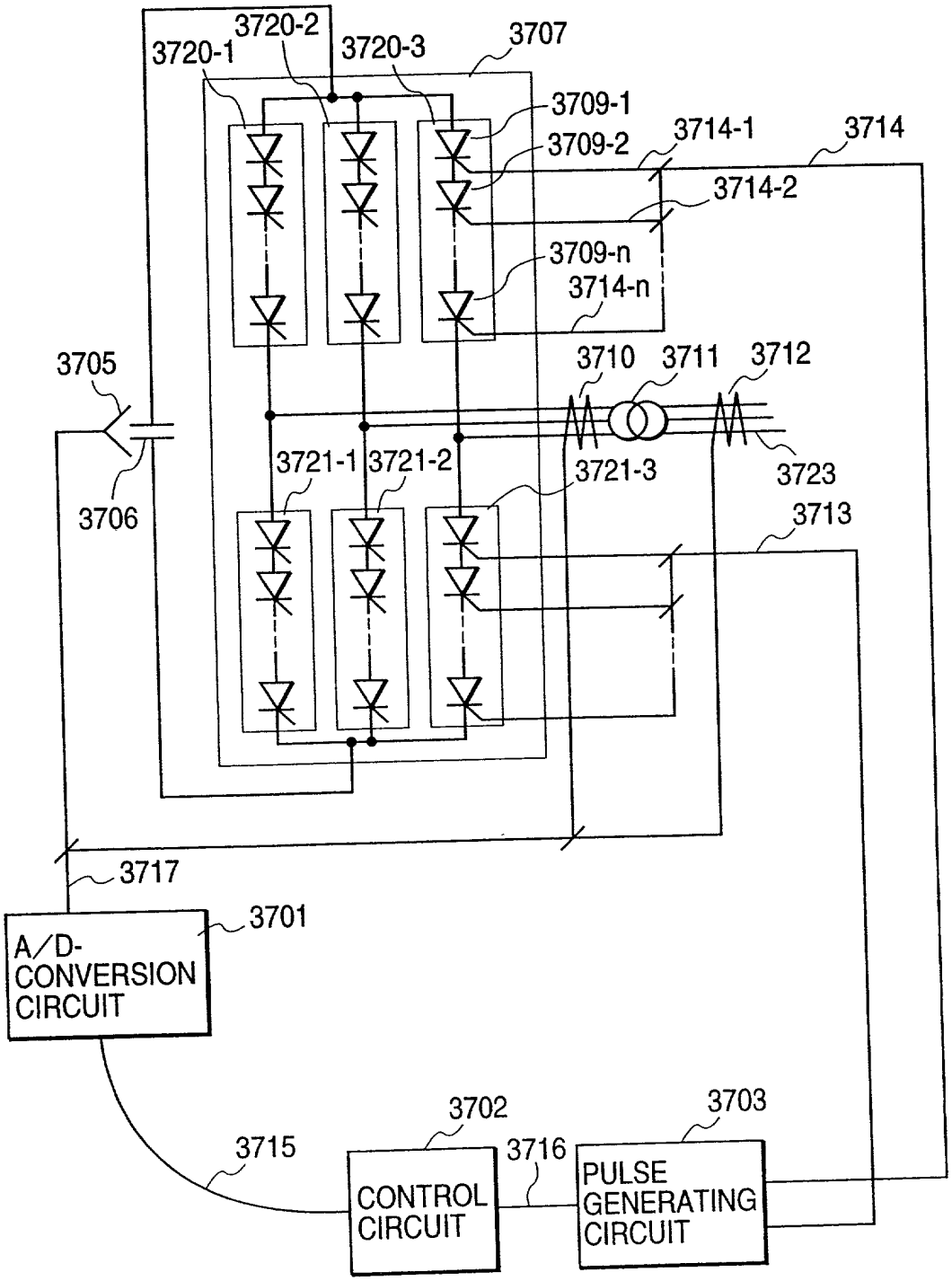

3720-1
3720-2
3720-3
3707
3709-1
3709-2
3714-1
3714
3714-2
3709-n
3714-n
3705
3710
3711
3712
3723
3706
3721-1
3721-2
3721-3
3713
3717
3701
A/D-
CONVERSION
CIRCUIT
3702
3703
3715
3716
CONTROL
CIRCUIT
PULSE
GENERATING
CIRCUIT

FIG. 38

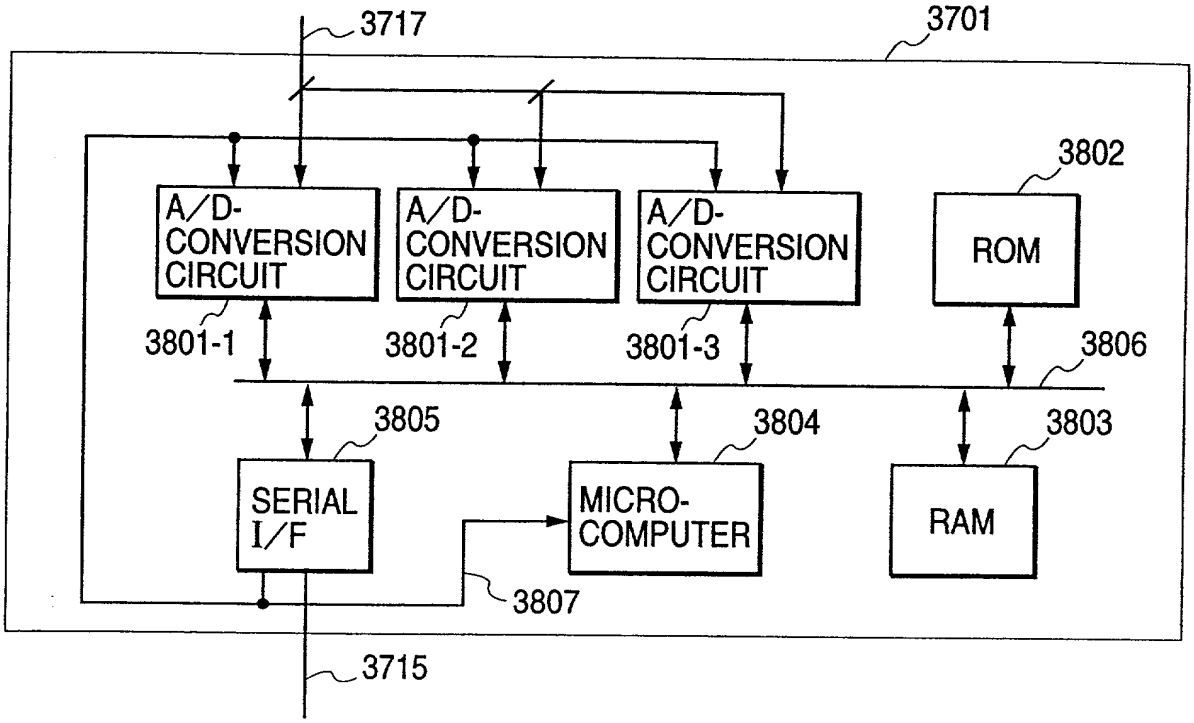

3717
3701
A/D-
CONVERSION
CIRCUIT
A/D-
CONVERSION
CIRCUIT
A/D-
CONVERSION
CIRCUIT
3802
ROM
3801-1
3801-2
3801-3
3806
3805
3804
3803
SERIAL
I/F
MICRO-
COMPUTER
RAM
3807
3715

FIG. 39

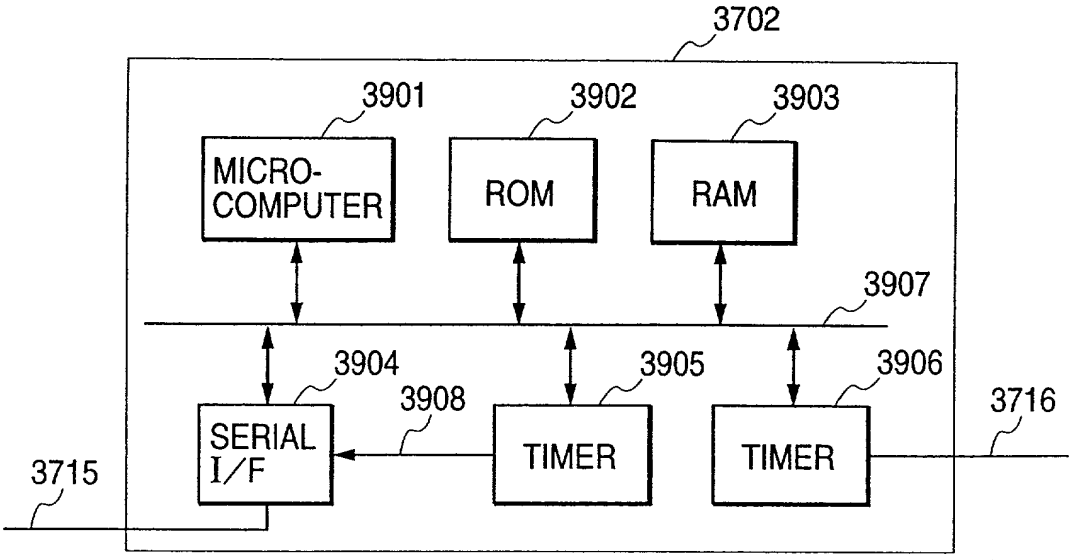

3702
3901
3902
3903
MICRO-
COMPUTER
ROM
RAM
3907
3904
3905
3906
3908
3716
SERIAL
I/F
TIMER
TIMER
3715

FIG. 40(a)

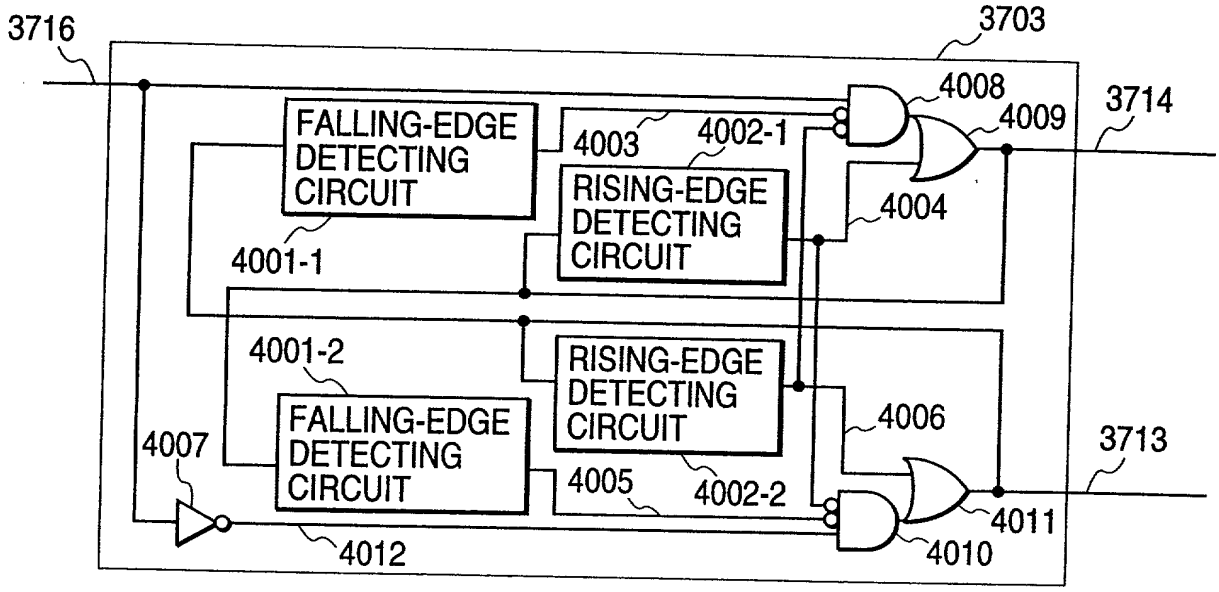


FIG. 40(b)

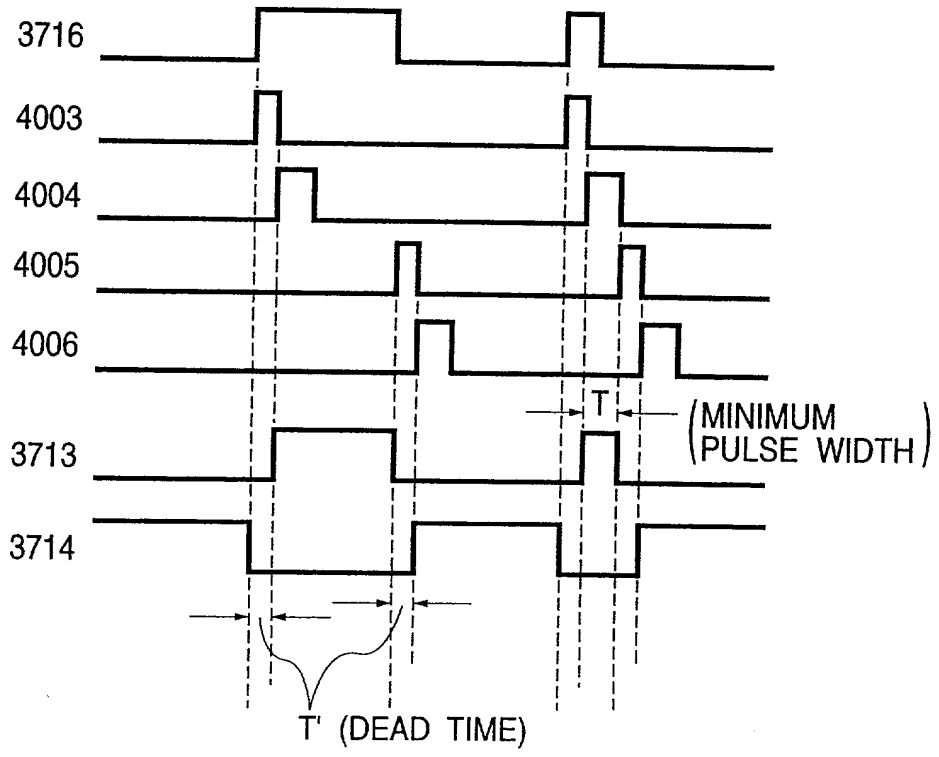


FIG. 41(a)

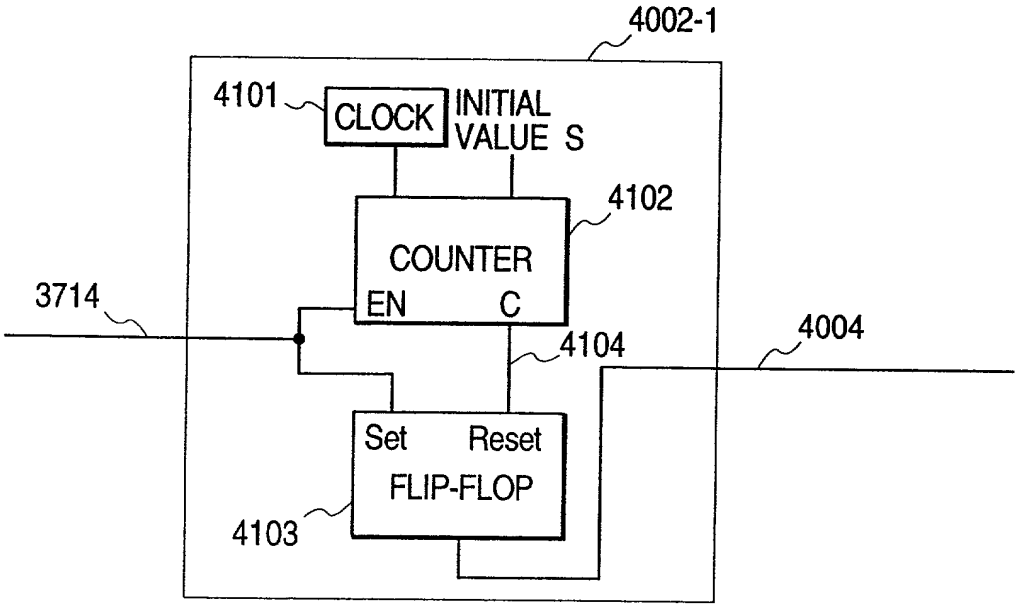


FIG. 41(b)

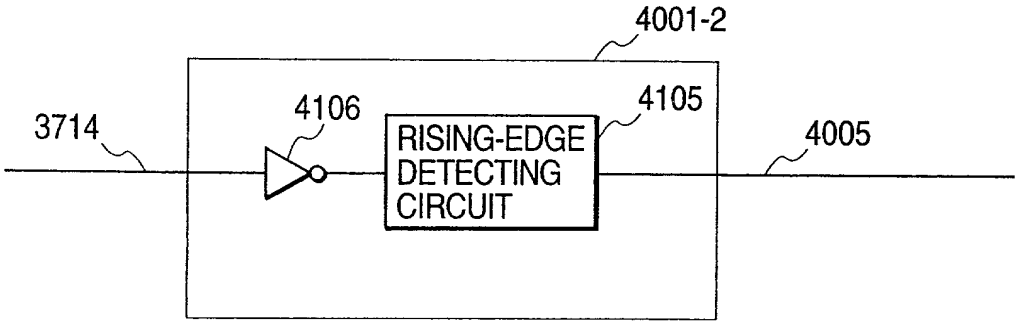


FIG. 42(a)

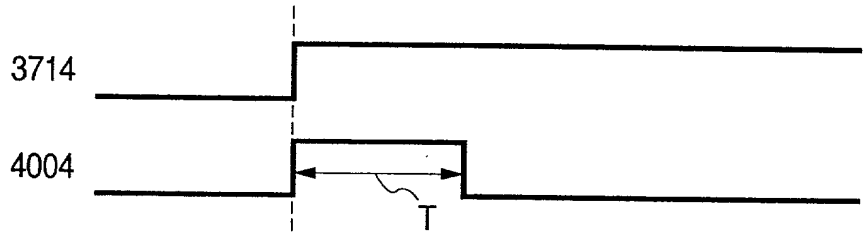


FIG. 42(b)

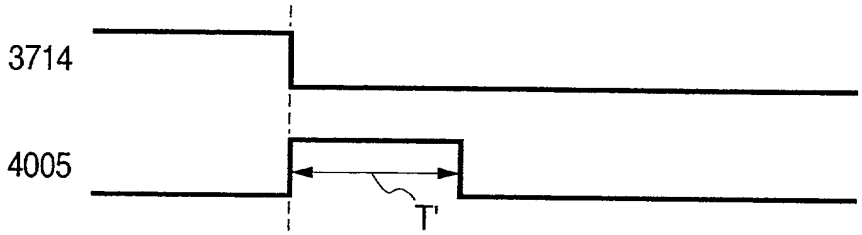


FIG. 43

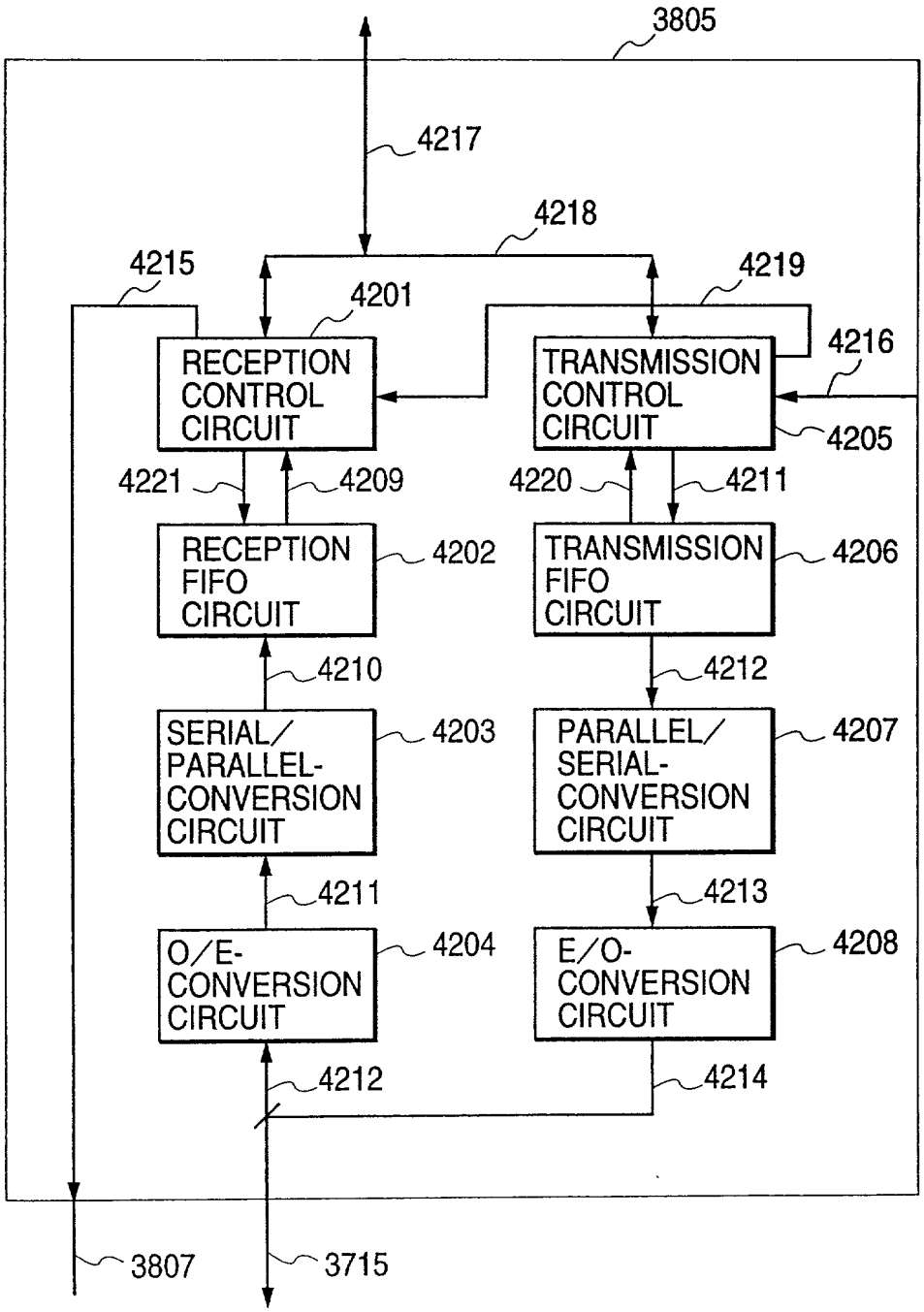

3805
4217
4218
4215
4219
4201
4216
RECEPTION CONTROL CIRCUIT
TRANSMISSION CONTROL CIRCUIT
4205
4221
4209
4220
4211
RECEPTION FIFO CIRCUIT
4202
TRANSMISSION FIFO CIRCUIT
4206
4210
4212
SERIAL/ PARALLEL-CONVERSION CIRCUIT
4203
PARALLEL/ SERIAL-CONVERSION CIRCUIT
4207
4211
4213
O/E-CONVERSION CIRCUIT
4204
E/O-CONVERSION CIRCUIT
4208
4212
4214
3807
3715

FIG. 44

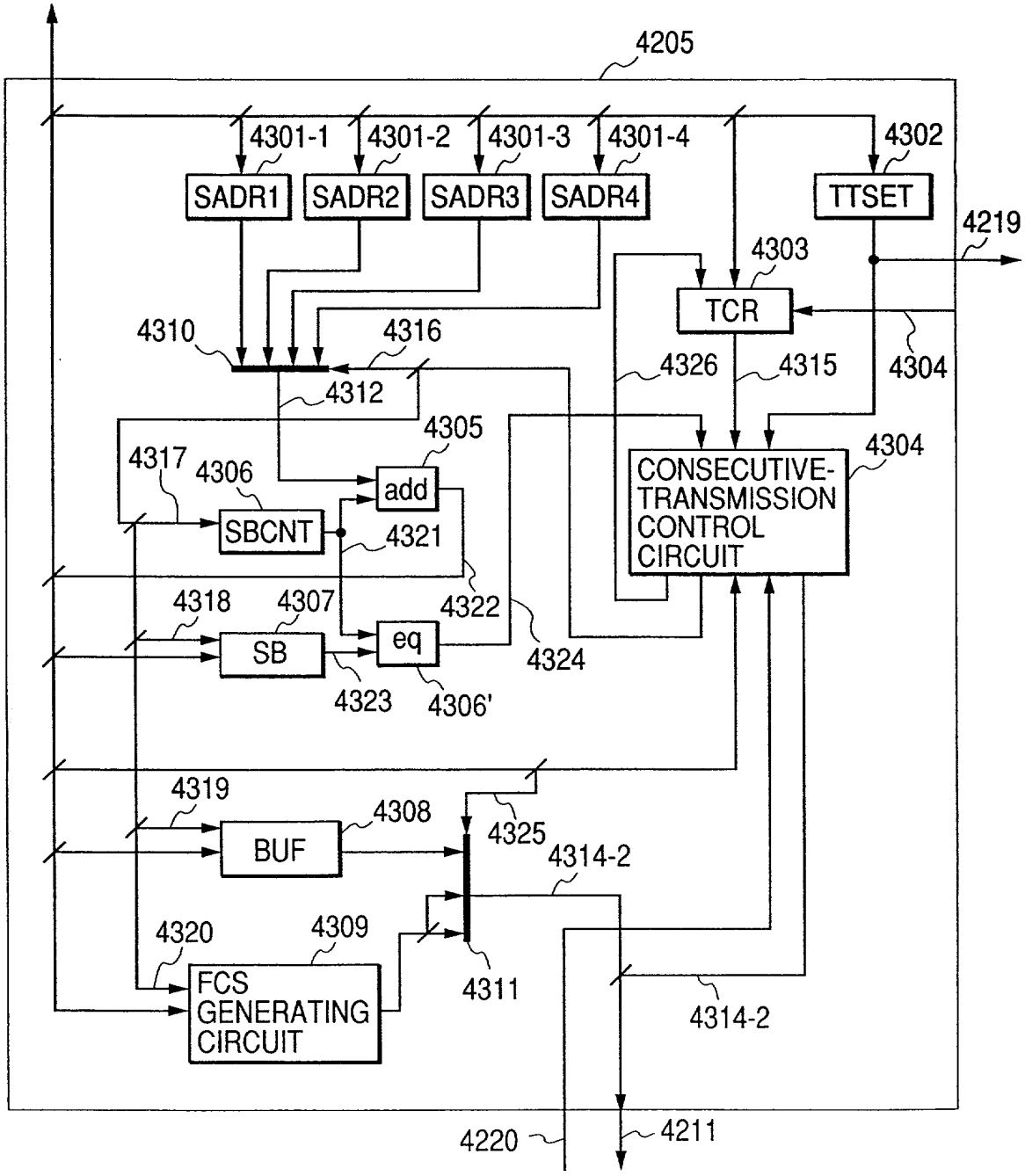

4205
4301-1
4301-2
4301-3
4301-4
4302
SADR1
SADR2
SADR3
SADR4
TTSET
4219
4303
TCR
4310
4316
4304
4326
4315
4312
4305
4304
4317
4306
add
CONSECUTIVE-TRANSMISSION CONTROL CIRCUIT
SBCNT
4321
4318
4307
4322
SB
eq
4324
4323
4306'
4319
4308
4325
BUF
4314-2
4320
4309
FCS GENERATING CIRCUIT
4311
4314-2
4220
4211

FIG. 45(a)

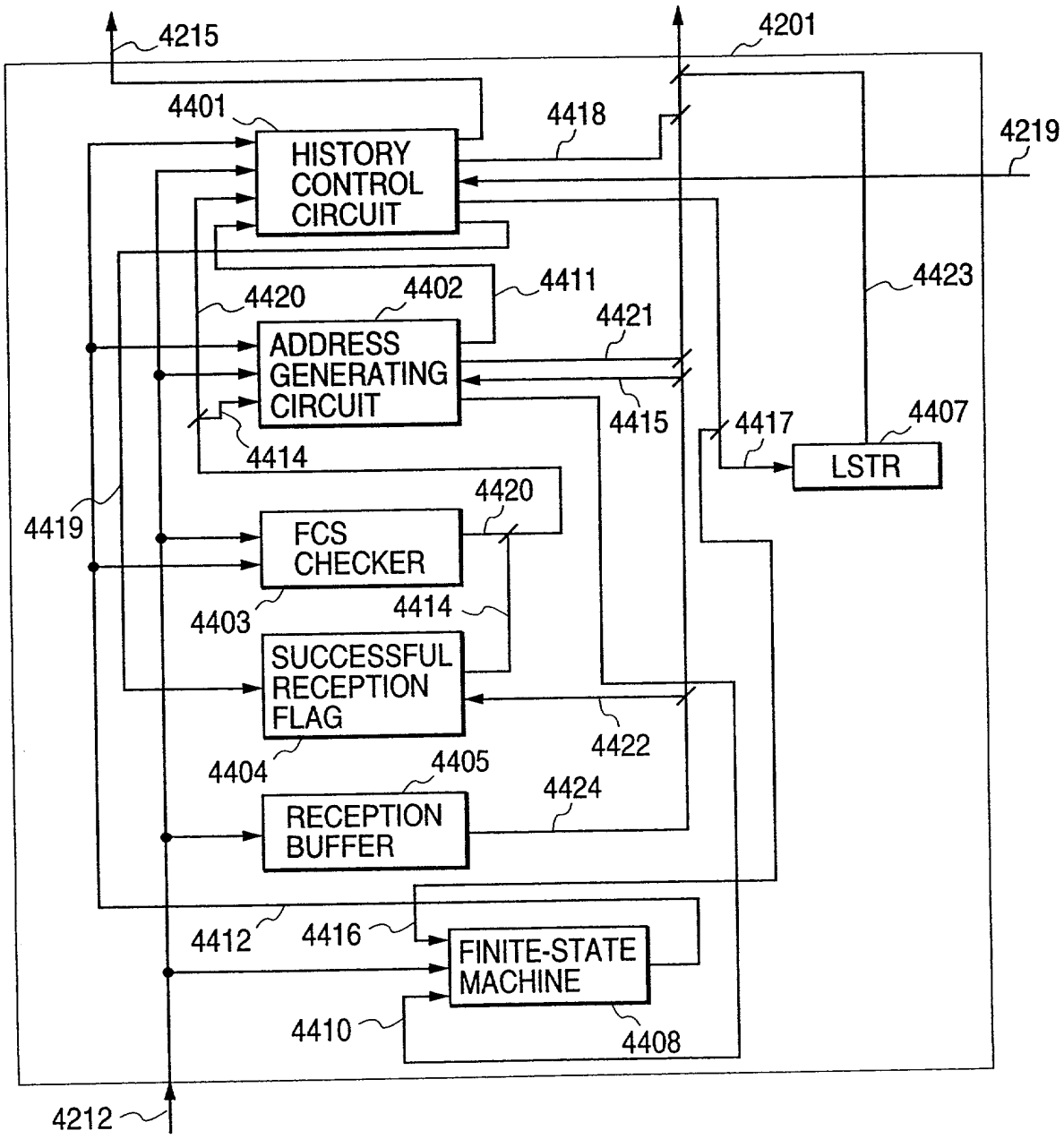


FIG. 45(b)

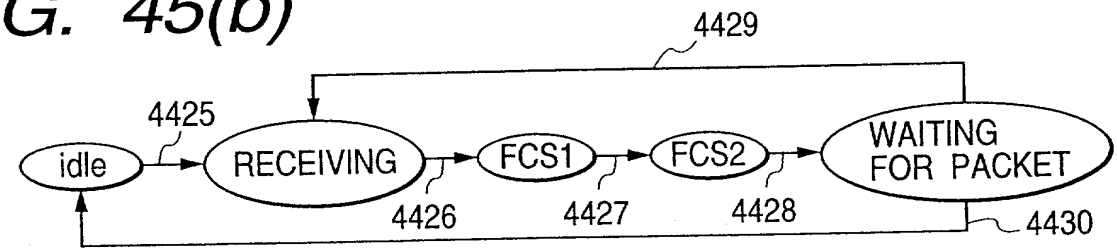


FIG. 46(a)

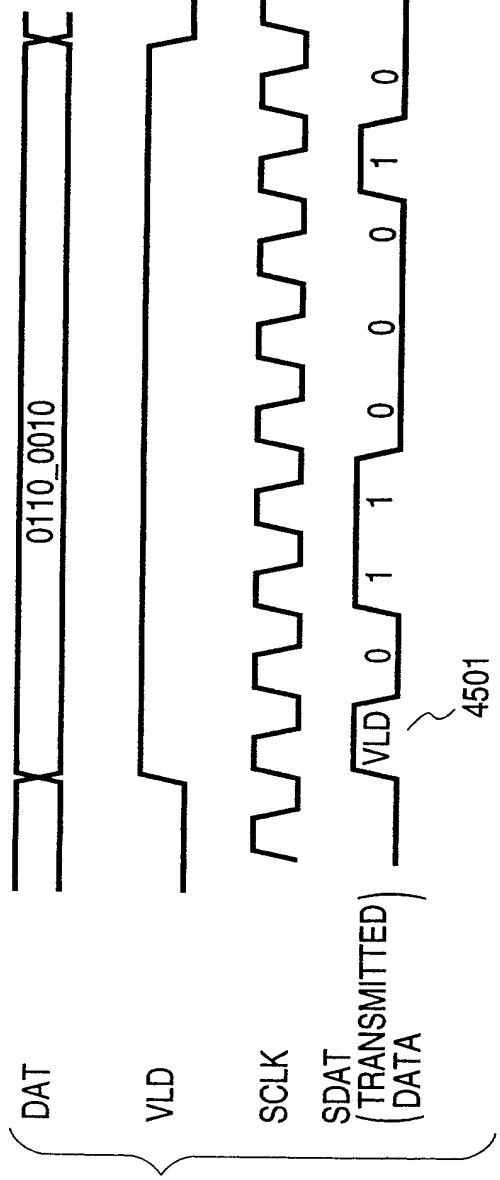


FIG. 46(b)

FIG. 47(a)

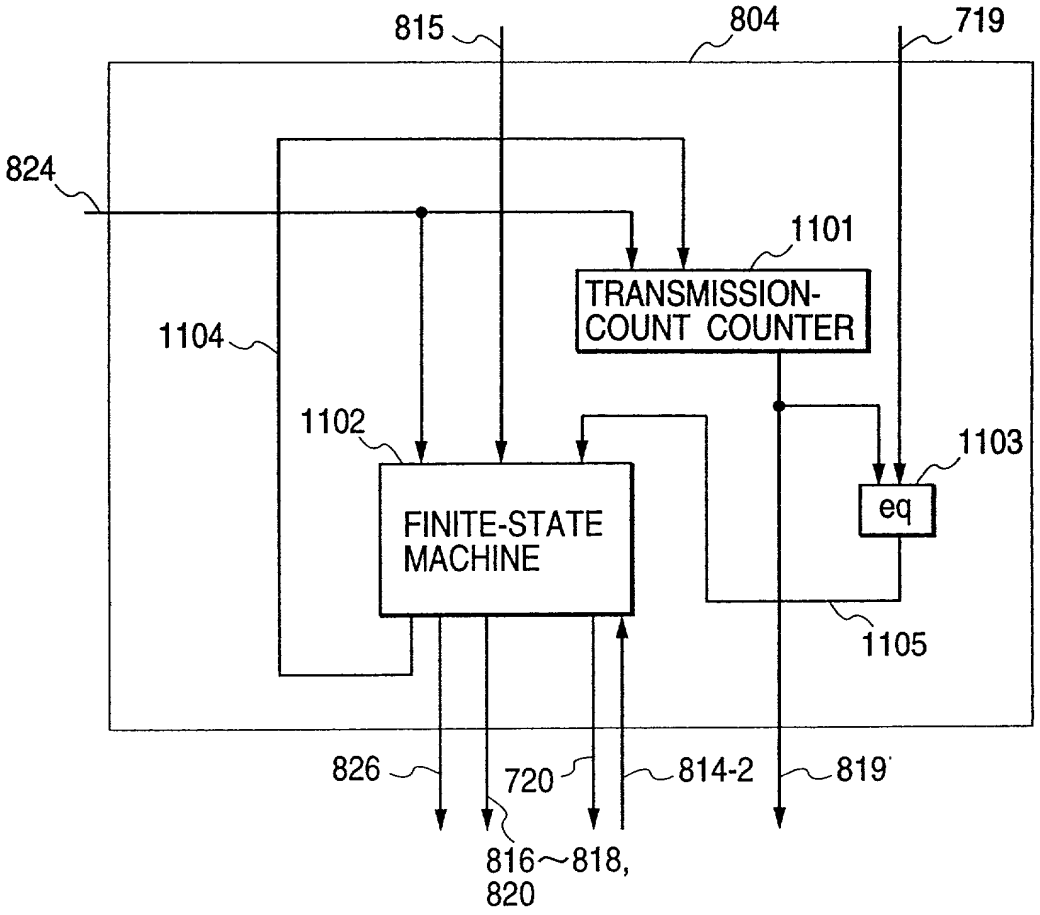


FIG. 47(a)

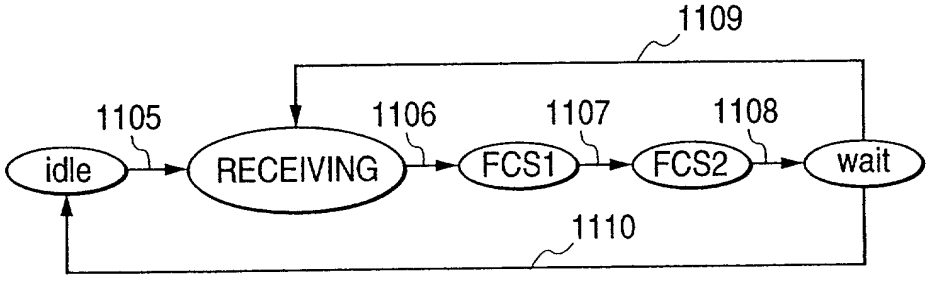


FIG. 48

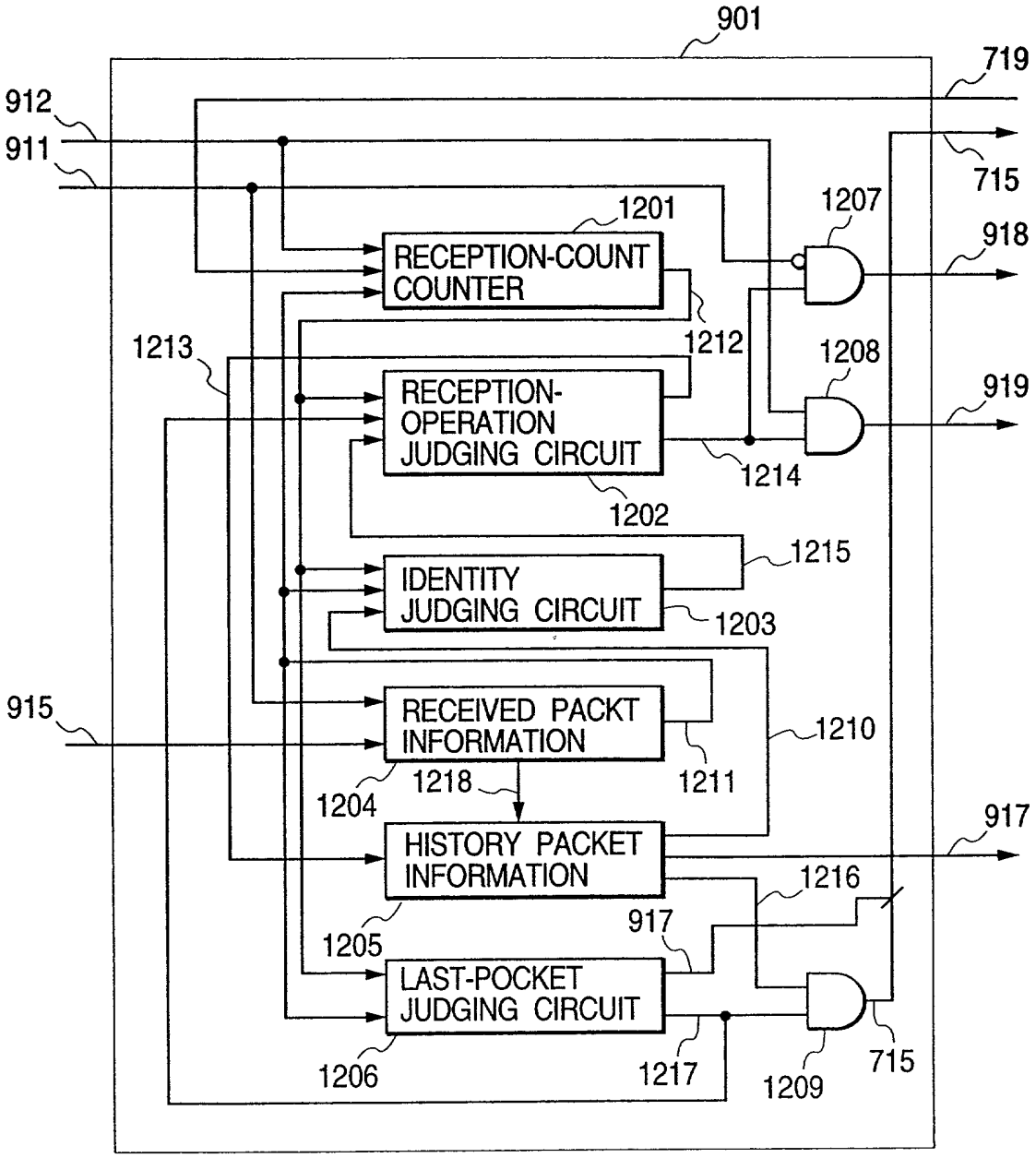

901
719
912
911
715
1201
1207
RECEPTION-COUNT COUNTER
918
1212
1213
1208
RECEPTION-OPERATION JUDGING CIRCUIT
919
1214
1202
1215
IDENTITY JUDGING CIRCUIT
1203
915
RECEIVED PACKT INFORMATION
1210
1211
1204
1218
917
HISTORY PACKET INFORMATION
1216
917
1205
LAST-POCKET JUDGING CIRCUIT
715
1206
1217
1209

FIG. 49

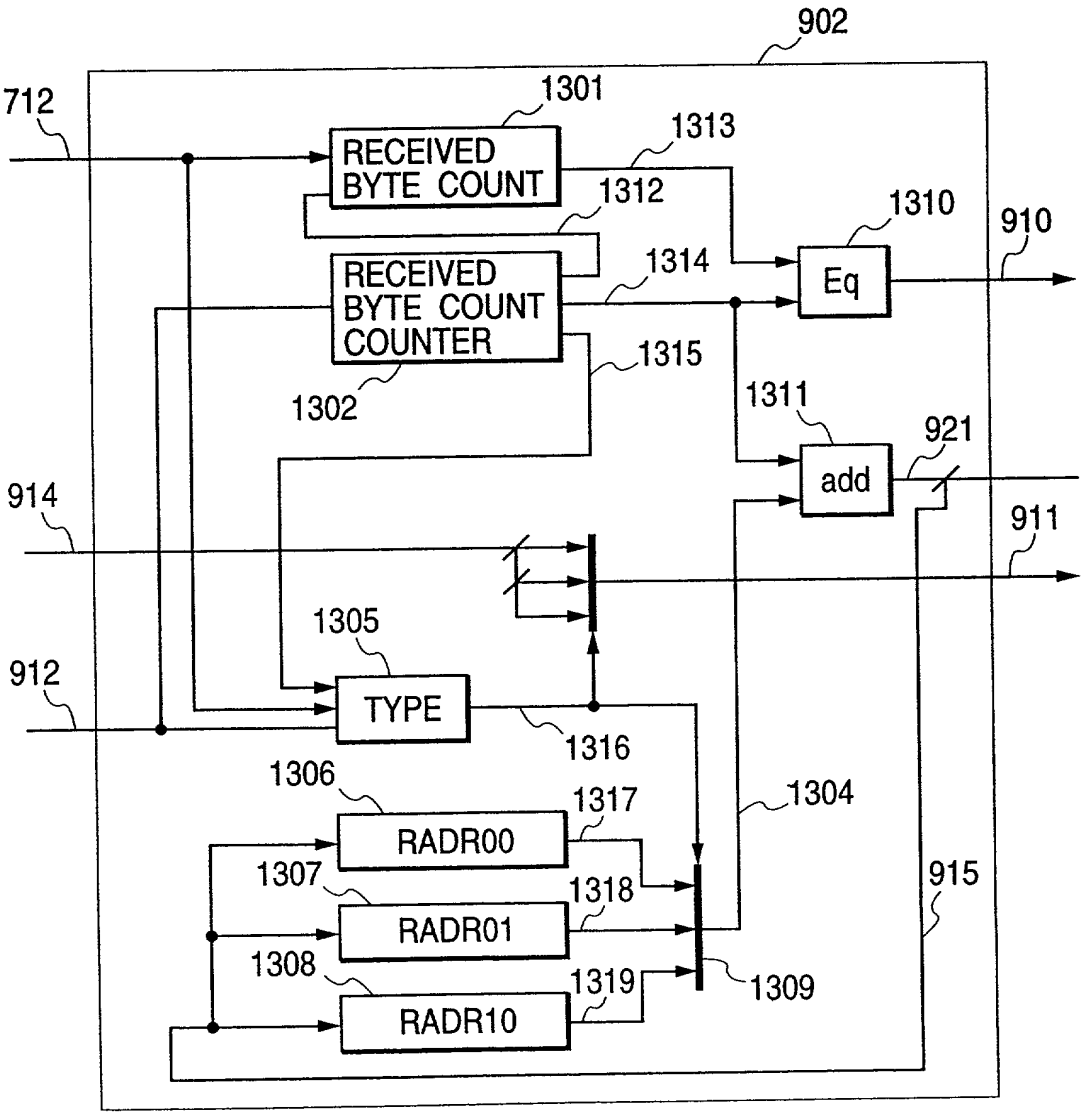

902
712
1301
RECEIVED BYTE COUNT
1313
1312
1310
910
RECEIVED BYTE COUNT COUNTER
1314
Eq
1315
1302
1311
921
add
914
911
1305
912
TYPE
1316
1306
1317
1304
RADR00
1307
1318
915
RADR01
1308
1319
1309
RADR10

FIG. 50(a)

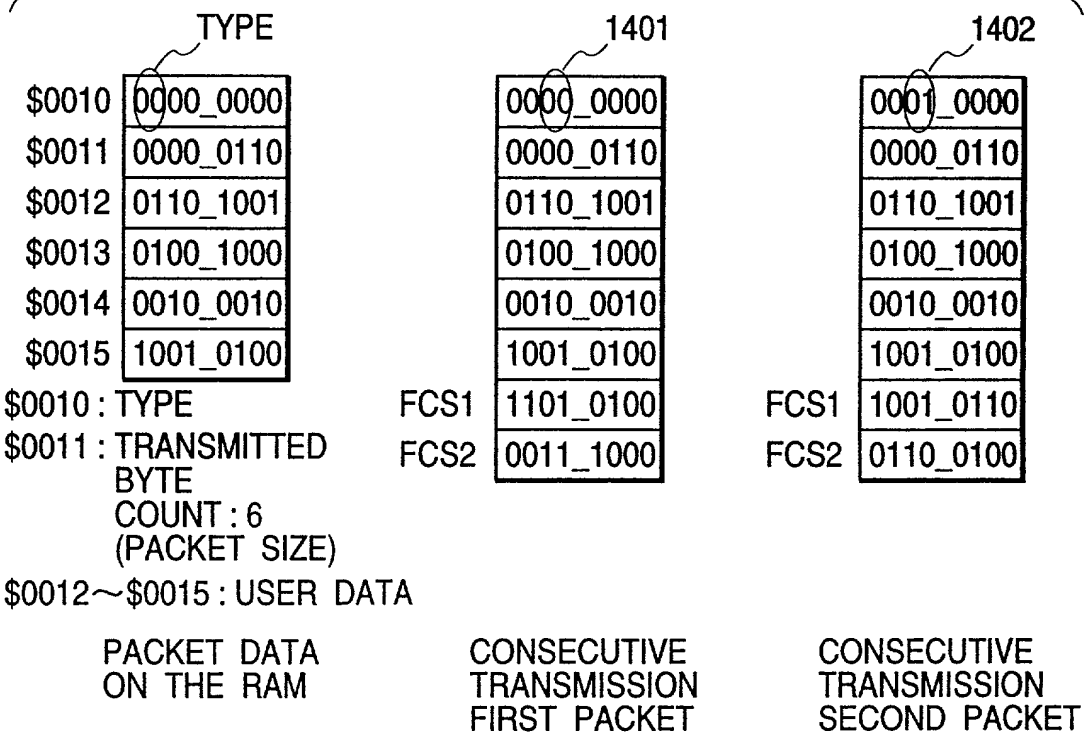


FIG. 50(b)

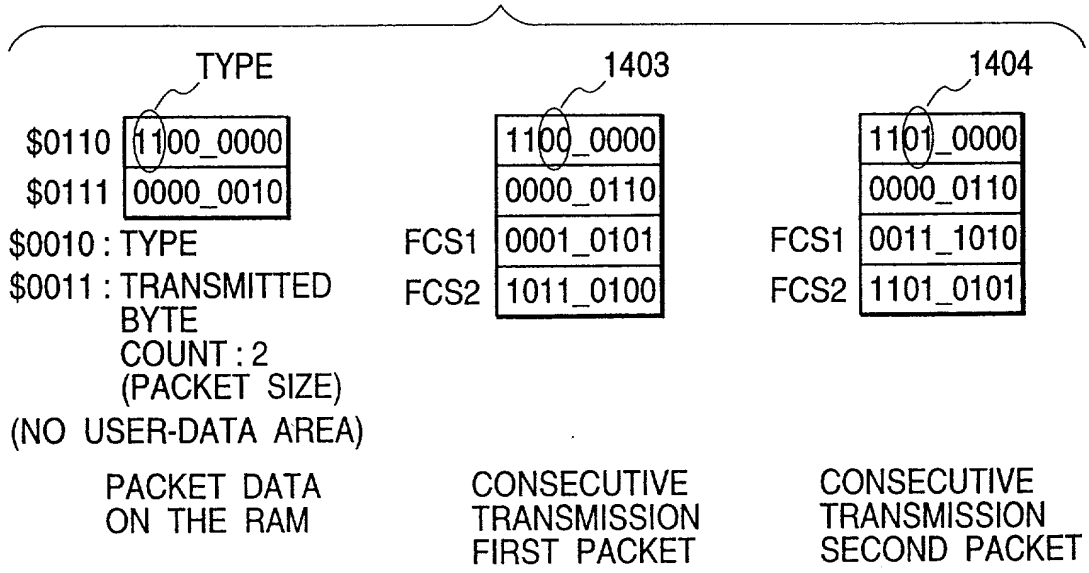


FIG. 51(a)

RECEPTION-OPERATION JUDGING CIRCUIT 4702
REQUEST FOR A MEMORY WRITE:
NO SUCCESSFUL HISTORY PACKET OF THE SAME TYPE IS RECEIVED IN THE PAST DURING RECEPTION OF DATA PACKETS.
REQUEST TO SET THE SUCCESSFUL-RECEPTION FLAG 4404:
NO ERROR RECORD EXISTS IN THE RECEIVED-PACKET-INFORMATION REGISTER 4704 AND (THE RECEPTION COUNT IN THE RECEPTION-COUNT COUNTER 4701=0 OR A RECORD OF AN ERROR EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 OR THE IDENTITY JUDGING CIRCUIT 4703 JUDGES A PACKET CURRENTLY BEING RECEIVED TO BE A PACKET OF A DIFFERENT TYPE).
ERROR-LOG REQUEST:
INFORMATION INDICATING DETECTION OF AN ERROR EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 AND A PACKET CURRENTLY BEING RECEIVED IS THE LAST ONE.
INTERRUPT SIGNAL TO THE SIGNAL LINE 4415:
THE TYPE OF A PACKET STORED IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 IS INDICATED BY A CODE OF '11' AND NO RECORD OF AN ERROR EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 AND A PACKET CURRENTLY BEING RECEIVED IS THE LAST ONE.

FIG. 51(b)

IDENTITY JUDGING CIRCUIT 4703:
NO ERROR EXISTS IN A PACKET CURRENTLY BEING RECEIVED AND THE RECEPTION COUNT IN THE RECEPTION-COUNT COUNTER 4701 IS NOT 0 AND (NO ERROR HISTORY EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 AND (THE PACKET TYPE RECORDED IN THE RECEIVED-PACKET-INFORMATION REGISTER 4704)=(THE PACKET TYPE RECORDED IN THE HISTORY-PACKET-INFORMATION REGISTER 4705) AND THE RECEPTION COUNT IN THE RECEPTION-COUNT COUNTER 4701<=THE SEQUENCE NUMBER n OF THE REPEATED TRANSMISSION OF THE PACKET CURRENTLY BEING RECEIVED) OR (AN ERROR HISTORY EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 AND THE RECEPTION COUNT IN THE RECEPTION-COUNT COUNTER 4701<=THE SEQUENCE NUMBER n OF THE REPEATED TRANSMISSION OF THE PACKET CURRENTLY BEING RECEIVED)

FIG. 51(c)

RECEIVED-PACKET-INFORMATION REGISTER 4704 HAVING A WIDTH OF 6 BITS:
- PACKET TYPE:2 BITS
- THE SEQUENCE NUMBER n OF THE REPEATED TRANSMISSION: 2 BITS
- ERROR INFORMATION-2 BITS:
  - ERROR TYPE: 1 BIT INDICATING A CRC ERROR OR A RECEIVED-DATA OVERRUN ERROR
  - ERROR DETECTION: 1 BIT INDICATING WHETHER AN ERROR IS DETECTED OR NOT

FIG. 51(d)

HISTORY-PACKET-INFORMATION REGISTER 4705 HAVING A WIDTH OF 4 BITS:
- PACKET TYPE: 2 BITS
- ERROR INFORMATION-2 BITS:
  - ERROR TYPE: 1 BIT INDICATING A CRC ERROR OR A RECEIVED-DATA OVERRUN ERROR
- ERROR DETECTION: 1 BIT INDICATING WHETHER AN ERROR IS DETECTED OR NOT

FIG. 51(e)

LAST-PACKET JUDGING CIRCUIT 4706:
(NO ERROR IS DETECTED IN A PACKET CURRENTLY BEING RECEIVED AND THE CONTENTS OF THE REPEATED-TRANSMISSION-COUNT SETTING REGISTER 4302)<=THE SEQUENCE NUMBER n OF THE REPEATED TRANSMISSION OF THE PACKET CURRENTLY BEING RECEIVED) AND (AN ERROR IS DETECTED IN A PACKET CURRENTLY BEING RECEIVED AND THE CONTENTS OF THE REPEATED-TRANSMISSION-COUNT SETTING REGISTER 4302<=THE CONTENTS OF THE RECEPTION-COUNTER 4701) OR (A SUCCESSFUL-RECEPTION HISTORY EXISTS IN THE HISTORY-PACKET-INFORMATION REGISTER 4705 AND THE PACKET TYPE STORED IN THE RECEIVED-PACKET-INFORMATION REGISTER 4704 IS DIFFERENT FROM THE PACKET TYPE STORED IN THE HISTORY-PACKET-INFORMATION REGISTER 4705) OR A TIME-OUT EVENT OCCURS DURING A PACKET WAITING STATE OF THE FINITE STATE MACHINE 4408.

FIG. 52

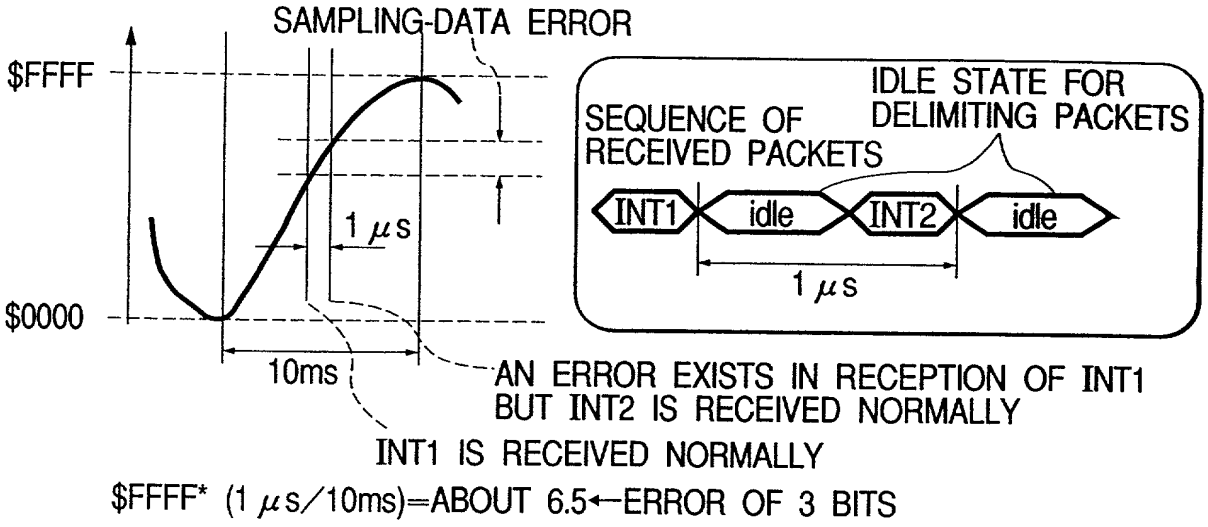

SAMPLING-DATA ERROR
$FFFF
$0000
1 μs
10ms
SEQUENCE OF RECEIVED PACKETS
IDLE STATE FOR DELIMITING PACKETS
INT1
idle
INT2
idle
1 μs
AN ERROR EXISTS IN RECEPTION OF INT1 BUT INT2 IS RECEIVED NORMALLY
INT1 IS RECEIVED NORMALLY
$FFFF* (1 μs/10ms)=ABOUT 6.5←ERROR OF 3 BITS

FIG. 54

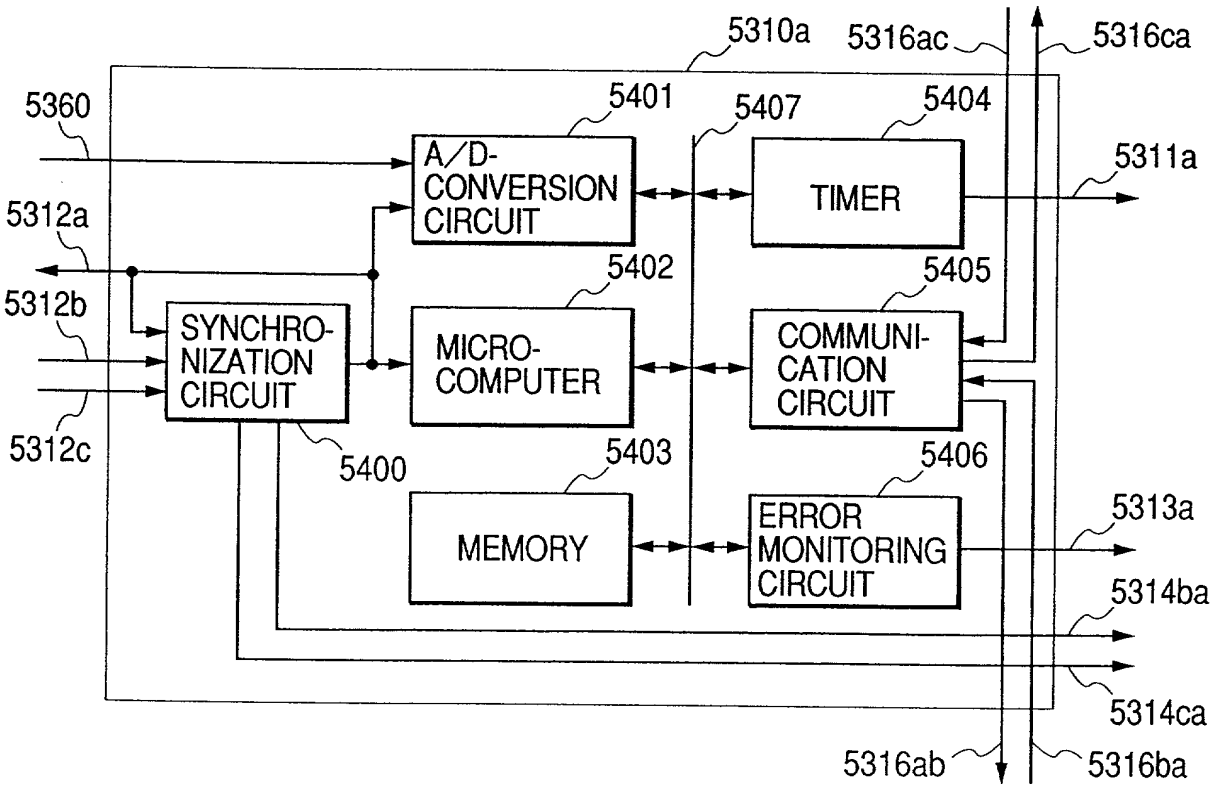

5310a
5316ac
5316ca
5360
5401
5407
5404
A/D-CONVERSION CIRCUIT
TIMER
5311a
5312a
5402
5405
5312b
SYNCHRO-NIZATION CIRCUIT
MICRO-COMPUTER
COMMUNI-CATION CIRCUIT
5312c
5400
5403
5406
MEMORY
ERROR MONITORING CIRCUIT
5313a
5314ba
5314ca
5316ab
5316ba

FIG. 53

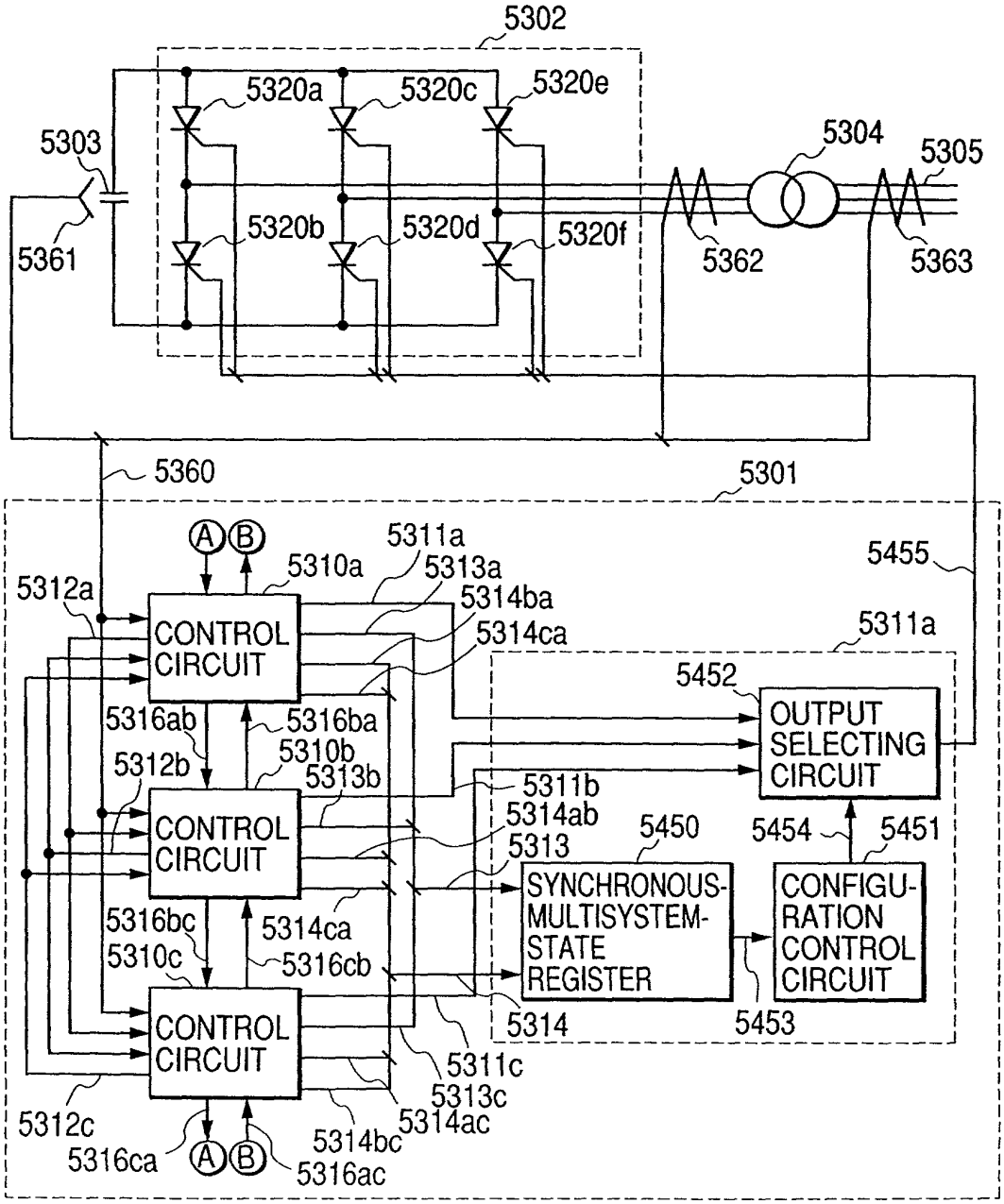

5302
5320a
5320c
5320e
5303
5304
5305
5320b
5320d
5320f
5361
5362
5363
5360
5301
A
B
5311a
5310a
5313a
5455
5312a
5314ba
5314ca
CONTROL CIRCUIT
5452
OUTPUT SELECTING CIRCUIT
5316ab
5316ba
5310b
5312b
5313b
5311b
5314ab
5313
5450
5454
5451
SYNCHRONOUS-MULTISYSTEM-STATE REGISTER
CONFIGU-RATION CONTROL CIRCUIT
5316bc
5314ca
5310c
5316cb
5314
5453
5311c
5313c
5314ac
5312c
5316ca
5314bc
5316ac

FIG. 55(a)

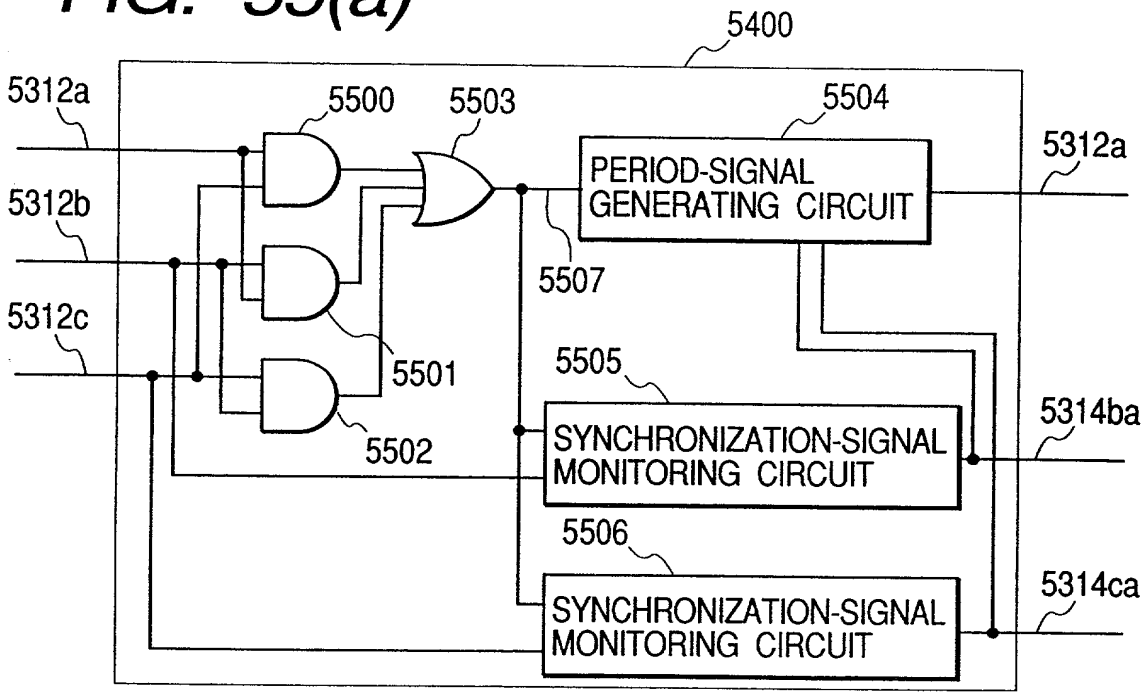


FIG. 56

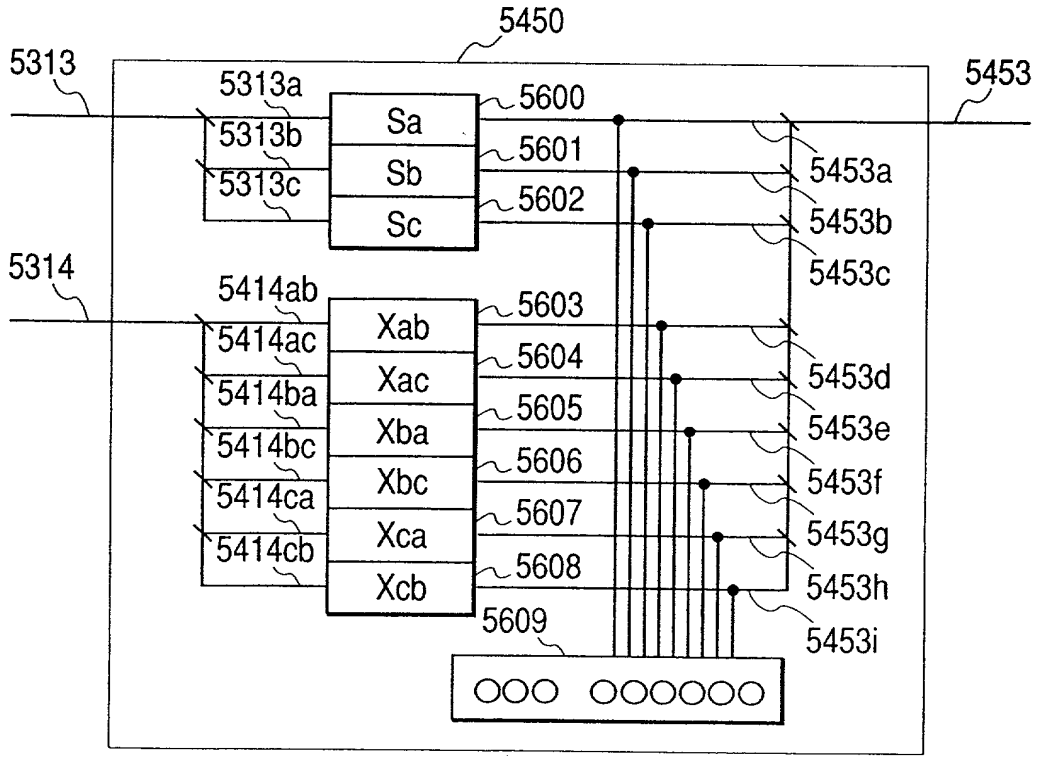


FIG. 55(b)

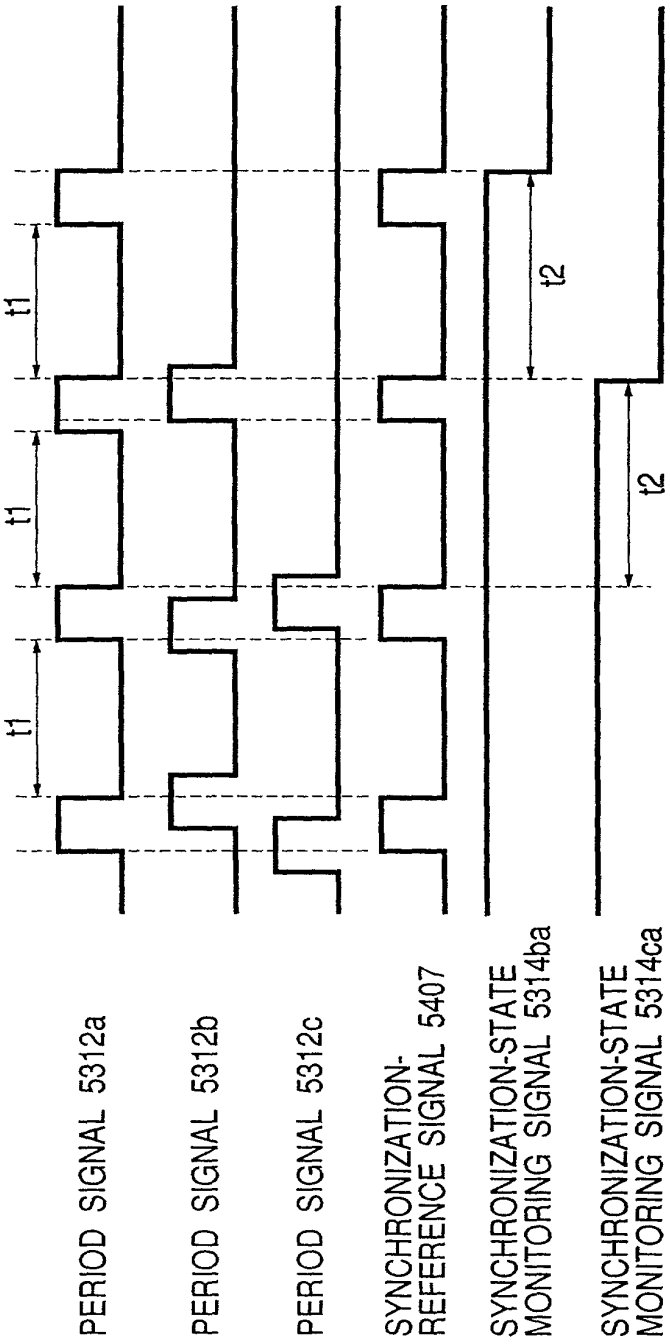

t1
t1
t1
t2
t2
PERIOD SIGNAL 5312a
PERIOD SIGNAL 5312b
PERIOD SIGNAL 5312c
SYNCHRONIZATION-REFERENCE SIGNAL 5407
SYNCHRONIZATION-STATE MONITORING SIGNAL 5314ba
SYNCHRONIZATION-STATE MONITORING SIGNAL 5314ca

FIG. 57

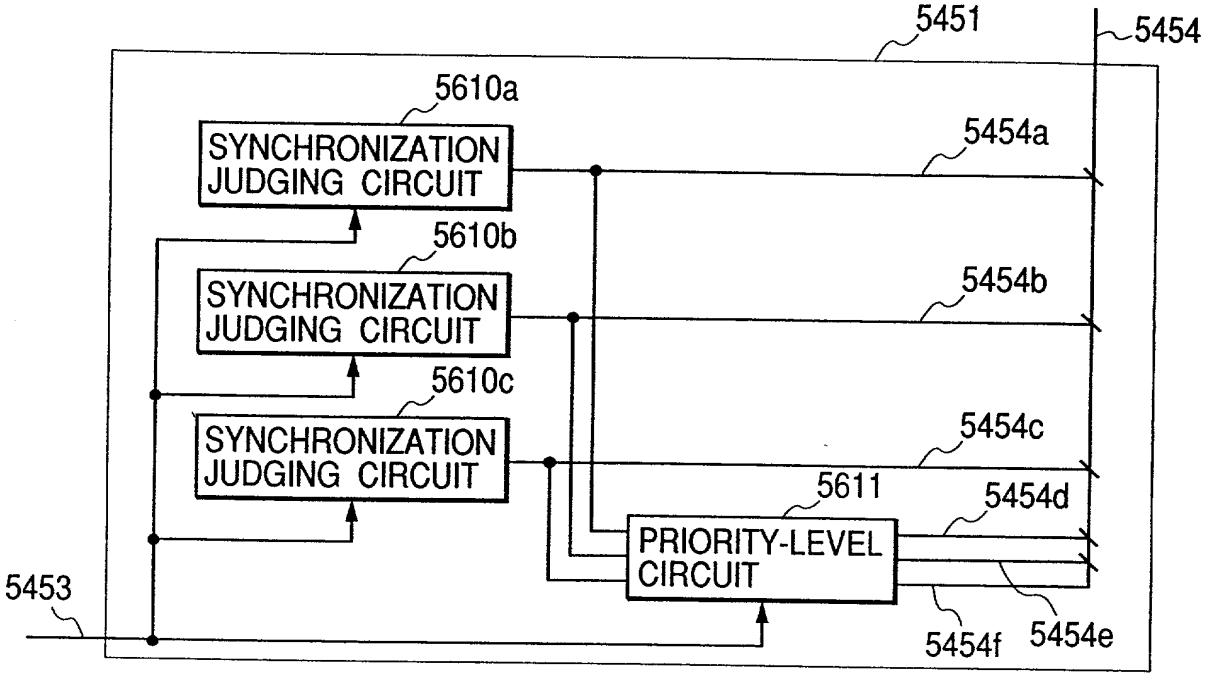

5451
5454
5610a
SYNCHRONIZATION JUDGING CIRCUIT
5454a
5610b
SYNCHRONIZATION JUDGING CIRCUIT
5454b
5610c
SYNCHRONIZATION JUDGING CIRCUIT
5454c
5611
PRIORITY-LEVEL CIRCUIT
5454d
5453
5454f
5454e

FIG. 59

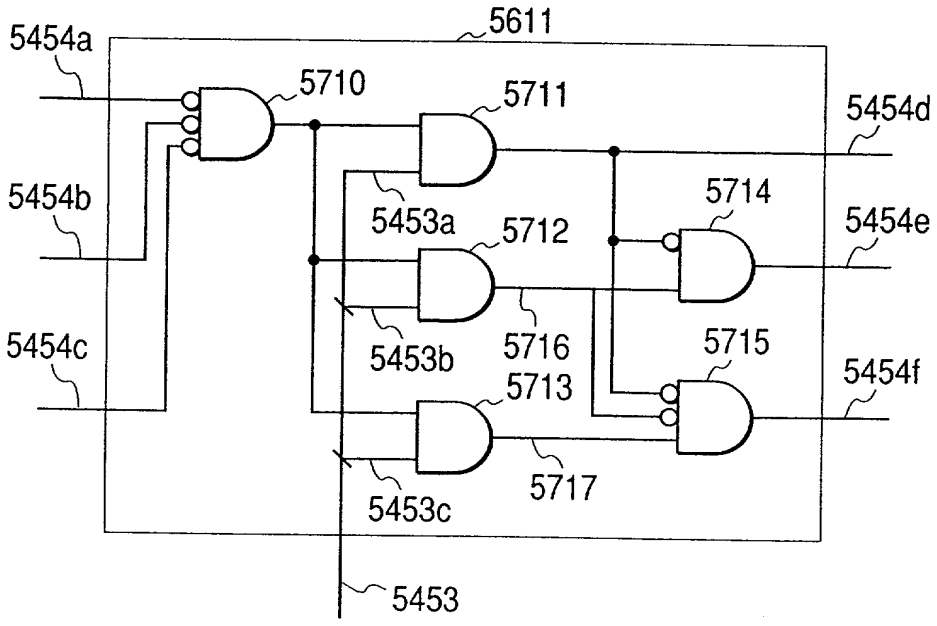

5611
5454a
5710
5711
5454d
5454b
5453a
5712
5714
5454e
5454c
5453b
5716
5715
5713
5454f
5717
5453c
5453

FIG. 58(a)

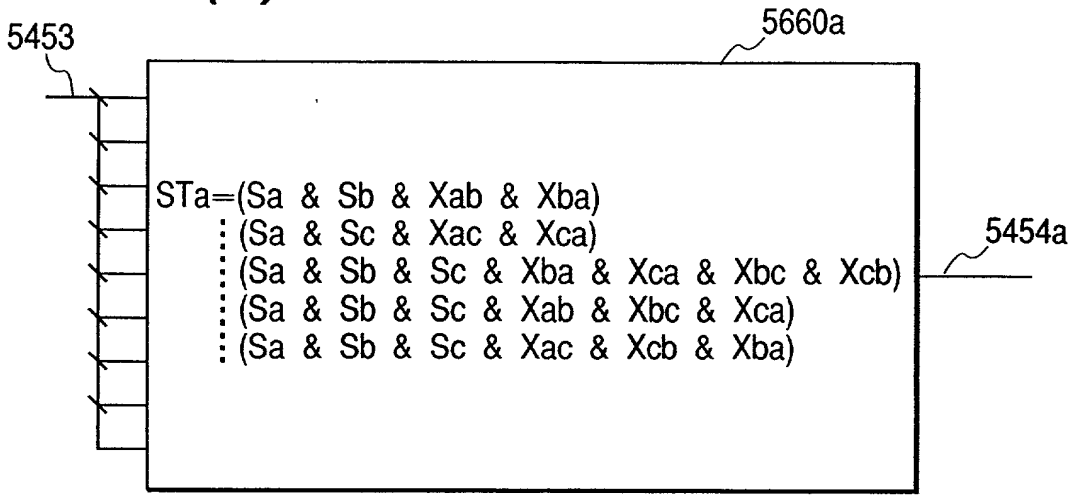


FIG. 58(b)

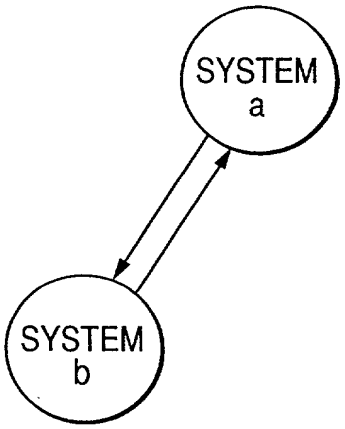


FIG. 58(c)

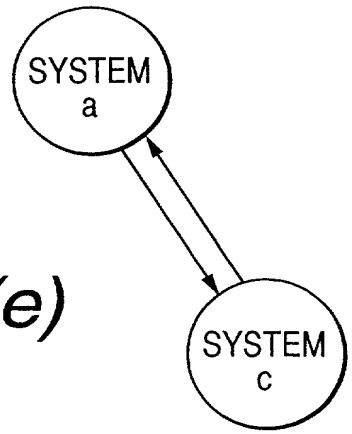


FIG. 58(d)

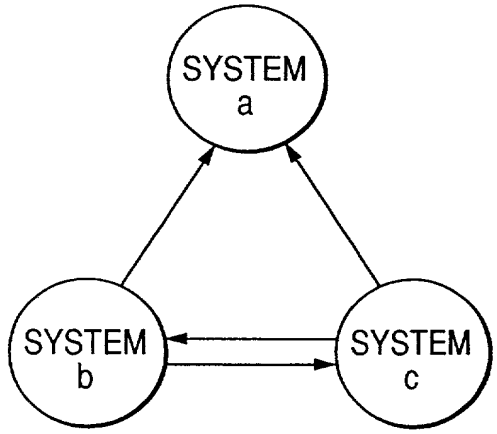


FIG. 58(e)

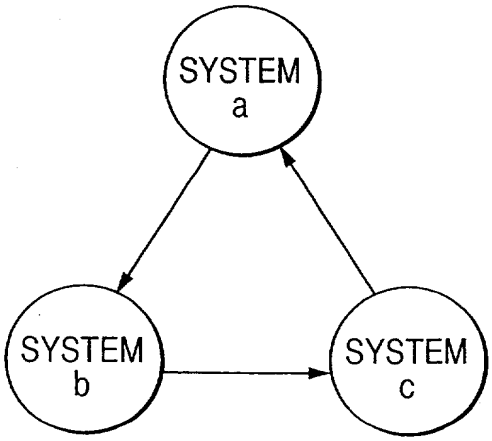


FIG. 58(f)

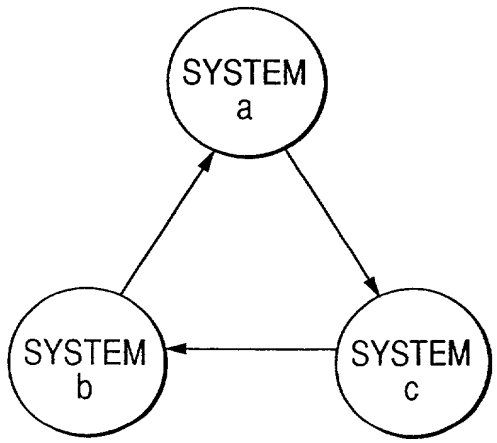


FIG. 60

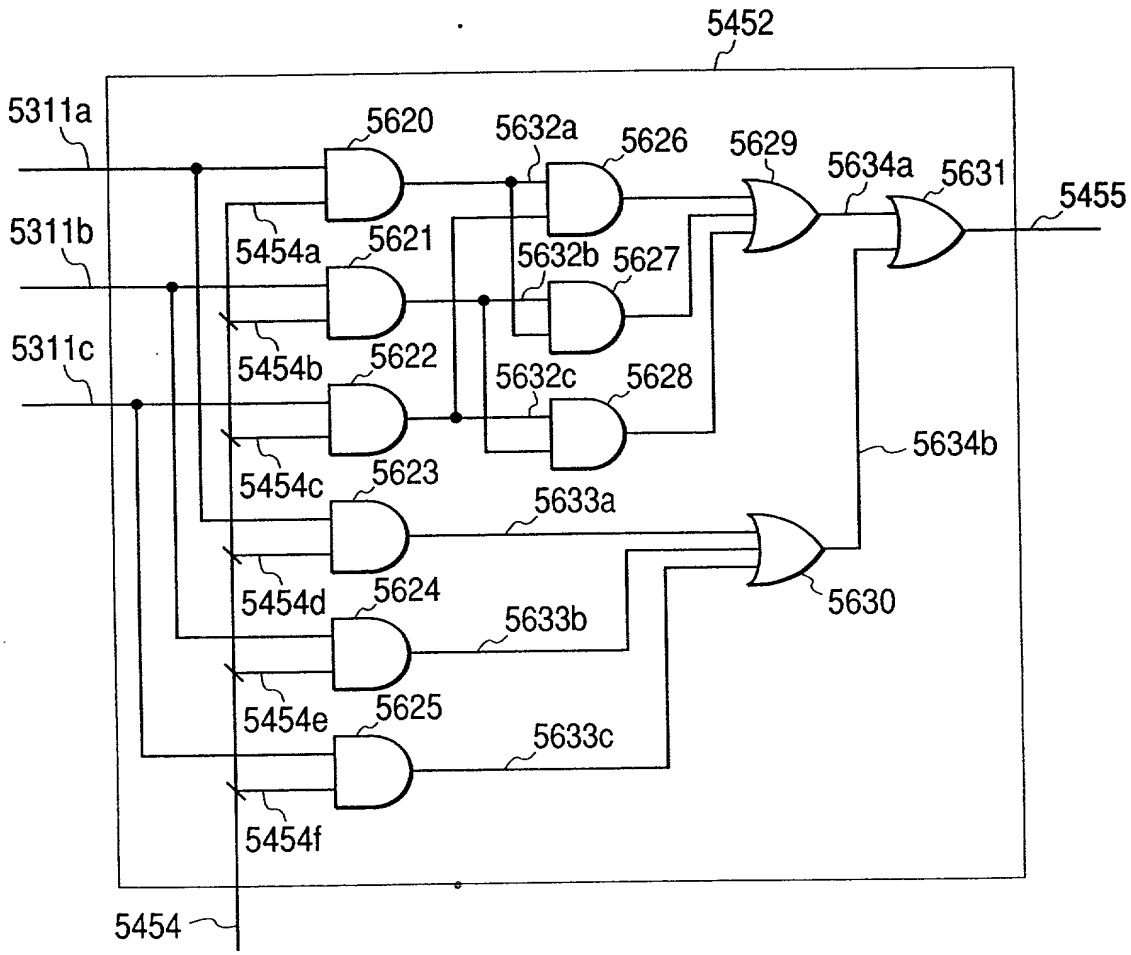

5452
5311a
5311b
5311c
5620
5621
5622
5623
5624
5625
5632a
5632b
5632c
5626
5627
5628
5629
5633a
5633b
5633c
5630
5634a
5634b
5631
5455
5454a
5454b
5454c
5454d
5454e
5454f
5454

FIG. 61

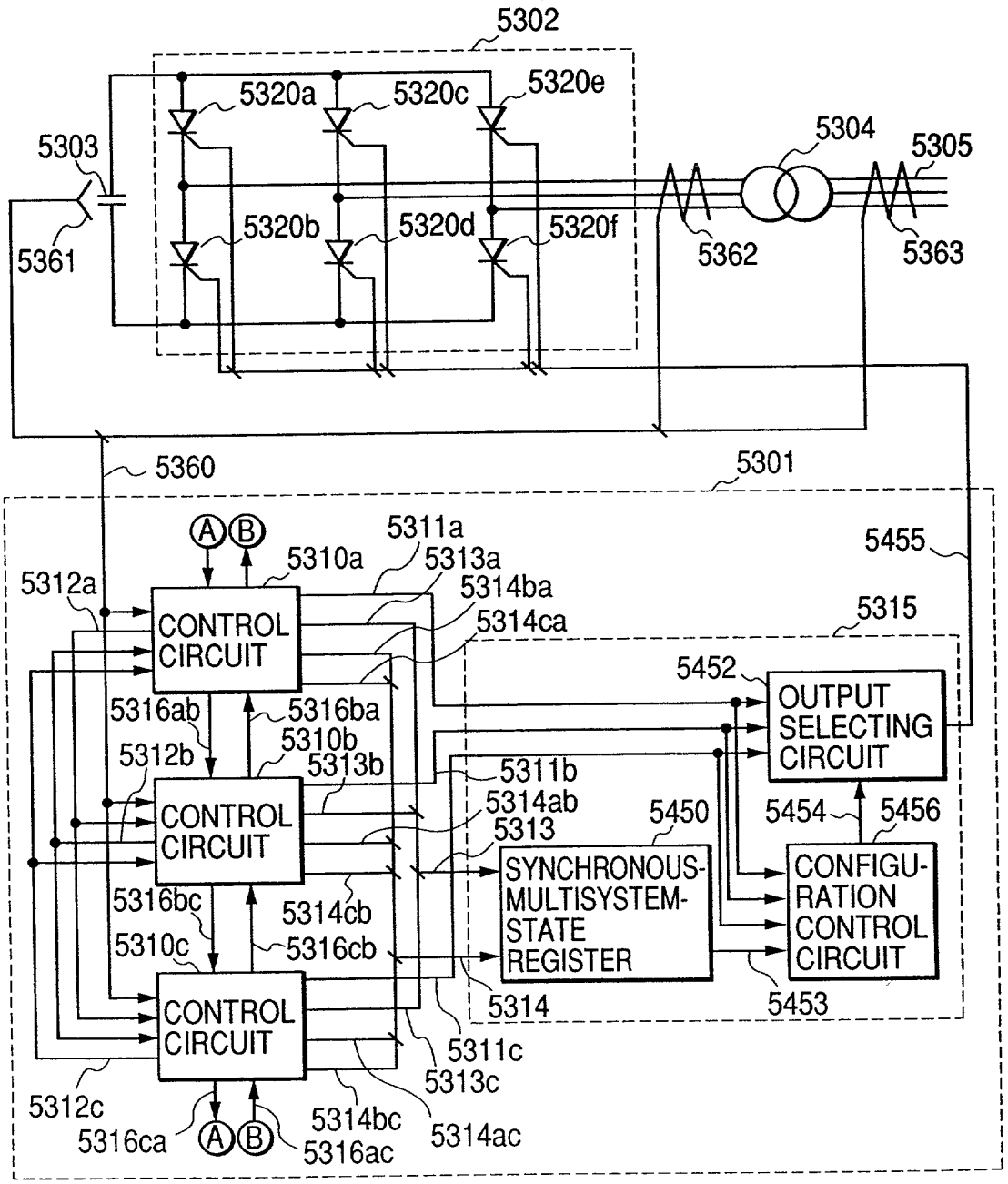

5302
5320a
5320c
5320e
5303
5304
5305
5320b
5320d
5320f
5361
5362
5363
5360
5301
A
B
5311a
5310a
5313a
5455
5312a
5314ba
5314ca
5315
CONTROL CIRCUIT
5452
OUTPUT SELECTING CIRCUIT
5316ab
5316ba
5310b
5312b
5313b
5311b
5314ab
5313
5450
5454
5456
CONTROL CIRCUIT
SYNCHRONOUS-MULTISYSTEM-STATE REGISTER
CONFIGU-RATION CONTROL CIRCUIT
5316bc
5314cb
5310c
5316cb
CONTROL CIRCUIT
5314
5453
5311c
5313c
5312c
5316ca
5314bc
5316ac
5314ac

FIG. 62

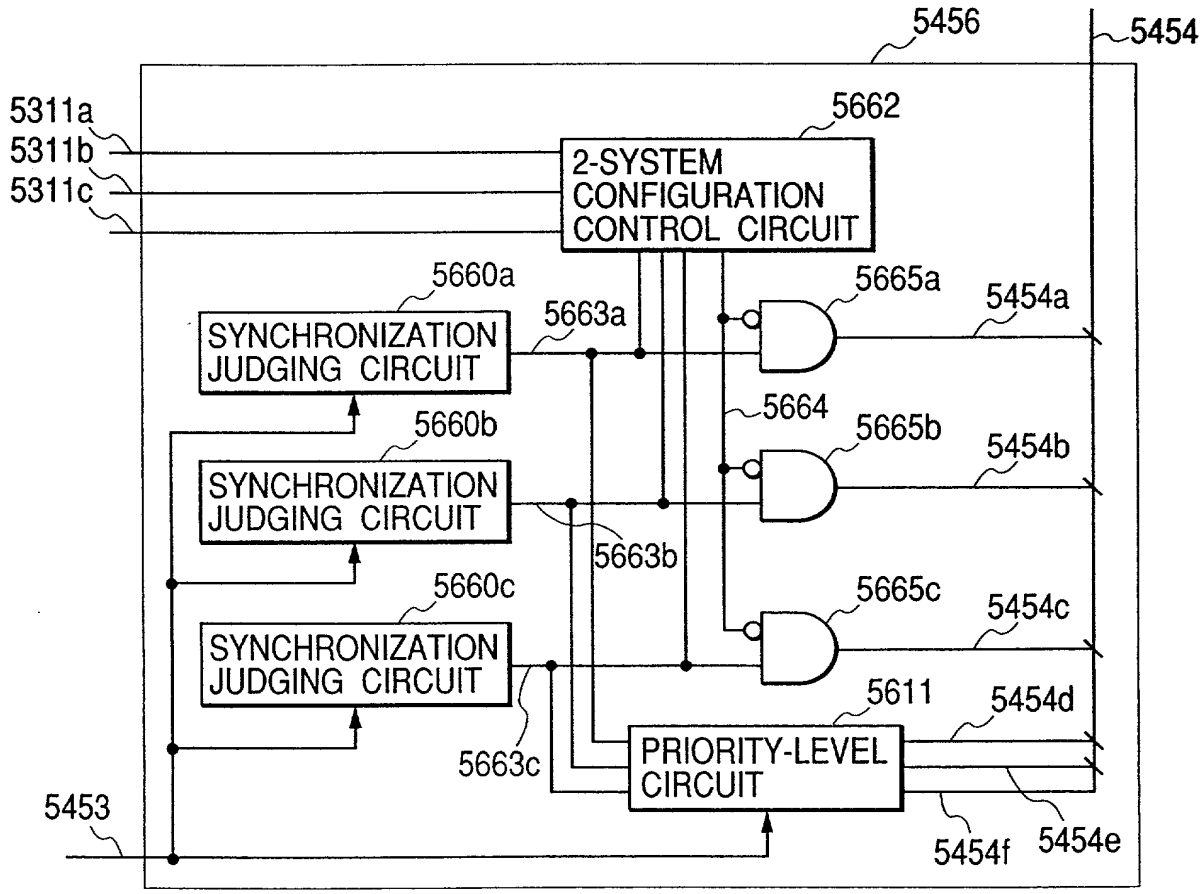

5456
5454
5311a
5311b
5311c
5662
2-SYSTEM CONFIGURATION CONTROL CIRCUIT
5660a
SYNCHRONIZATION JUDGING CIRCUIT
5663a
5665a
5454a
5660b
SYNCHRONIZATION JUDGING CIRCUIT
5664
5665b
5454b
5663b
5660c
SYNCHRONIZATION JUDGING CIRCUIT
5665c
5454c
5611
5454d
PRIORITY-LEVEL CIRCUIT
5663c
5453
5454f
5454e

FIG. 63(a)

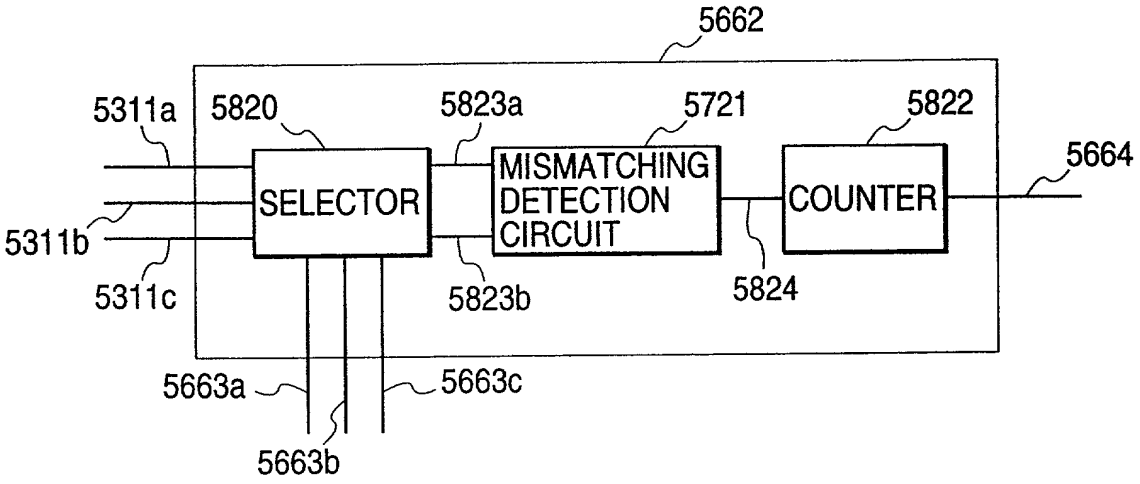


FIG. 63(b)

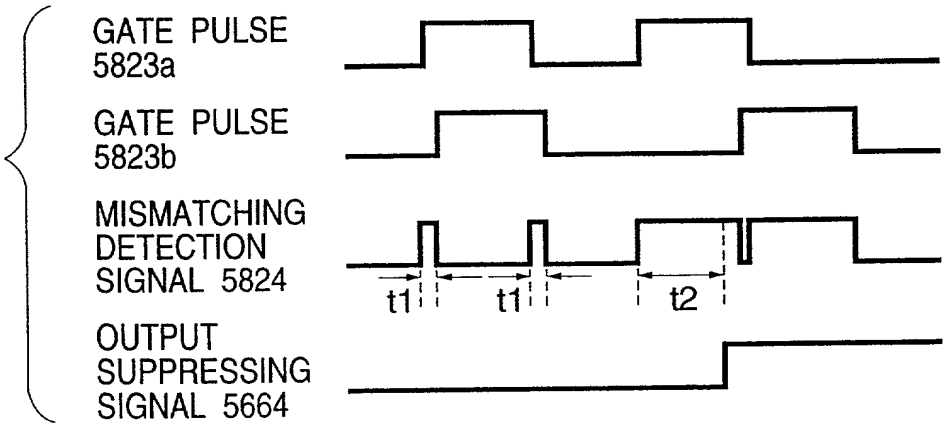


FIG. 64(a)

SELECTOR 5820

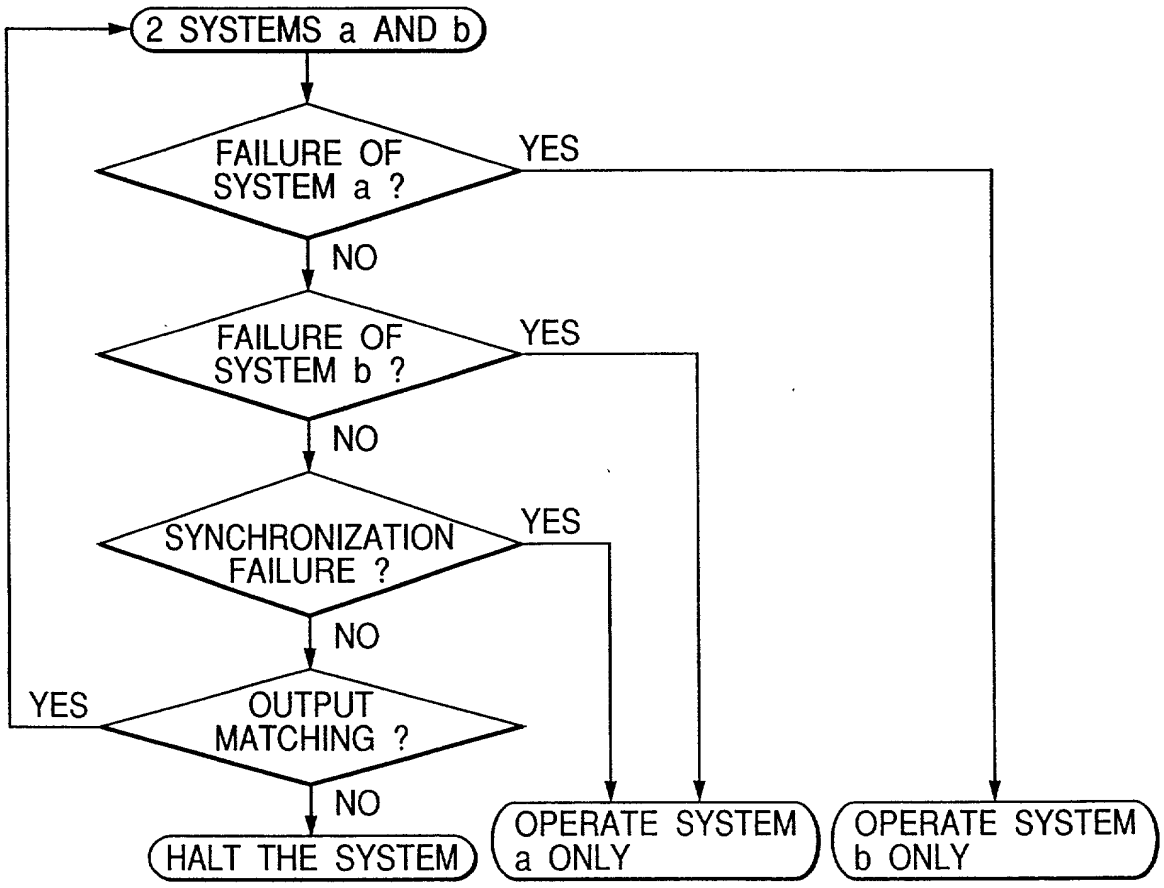
5663a	5663b	5663c	5823a	5823b
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	11b	11c
1	0	0	0	0
1	0	1	11a	11c
1	1	0	11a	11b
1	1	1	0	0

FIG. 64(b)

MISMATCHING DETECTION CIRCUIT 5821

5823a	5823b	5824
0	0	0
0	1	1
1	0	1
1	1	0

FIG. 65


2 SYSTEMS a AND b
FAILURE OF SYSTEM a ?
YES
NO
FAILURE OF SYSTEM b ?
YES
NO
SYNCHRONIZATION FAILURE ?
YES
NO
YES
OUTPUT MATCHING ?
NO
HALT THE SYSTEM
OPERATE SYSTEM a ONLY
OPERATE SYSTEM b ONLY